Control system and DAQ system using Real time computers and Analog electronics

KAGRA Program Advisory Board
@ Toyama University
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Objectives

- DGS (DiGital control System):
  - provides a platform to establish control systems for an interferometer and subsystems of KAGRA.
  - provides a DAQ (data acquisition) system.
  - provides many flexible functions like monitors/ diagnostics/human interfaces.
- AEL (Analog ELectronics):
  - manufactures necessary circuits for subsystems of KAGRA.
  - connects subsystem and computers for flexible control .

DGS (DiGital control System)

- Provided real time control software from LIGO.
- Constructed hardware and networks step by step at Kamioka site.
  A. 2009-2010 prototype test @ CLIO
     – Basic IFO operation and noise performance
  B. 2010~ standalone system for KAGRA subsystems
  C. 2011 Small network test with 1 master and 2 RT PCs
  D. 2012-2013 Full test@ Kamioka new building
     – Closer to real scale PCs and network

System upgrade

	Stand alone FY2010-	Small network FY2011	Large network FY2012, 2013	Full system FY2014~
Real time PC	1	2	5	~30
IO chassis	1	2	5	~30
ADC	1	2	~10	~65
DAC	1	1	~10	~45
Binary Output	1	0	~10	~85
Long distance RFM	0	1	2	3
Short distance RFM	0	1	2	2
DAQ network switch	0	1	4	4
Timing switch	0	1	3	3
Boot server	0	1	3	3
Network file system		0	1	1
Build server	0	0	1	1
NAT	0	0	2	2
Data concentrator	0	0	1	1
NDS distributer	0	0	2 (redundant)	2 (redundant)
Frame writer	0	0	2 (redundant)	4 (redundant)
IRIG-B switch	0	0	1	3
Data storage	1TB (local)	1TB (local)	~20TB x2 (ext.)	~200TB (ext.)

Red: New items Green: increment

Computer room
in the mine

Diagram of KAGRA controls system

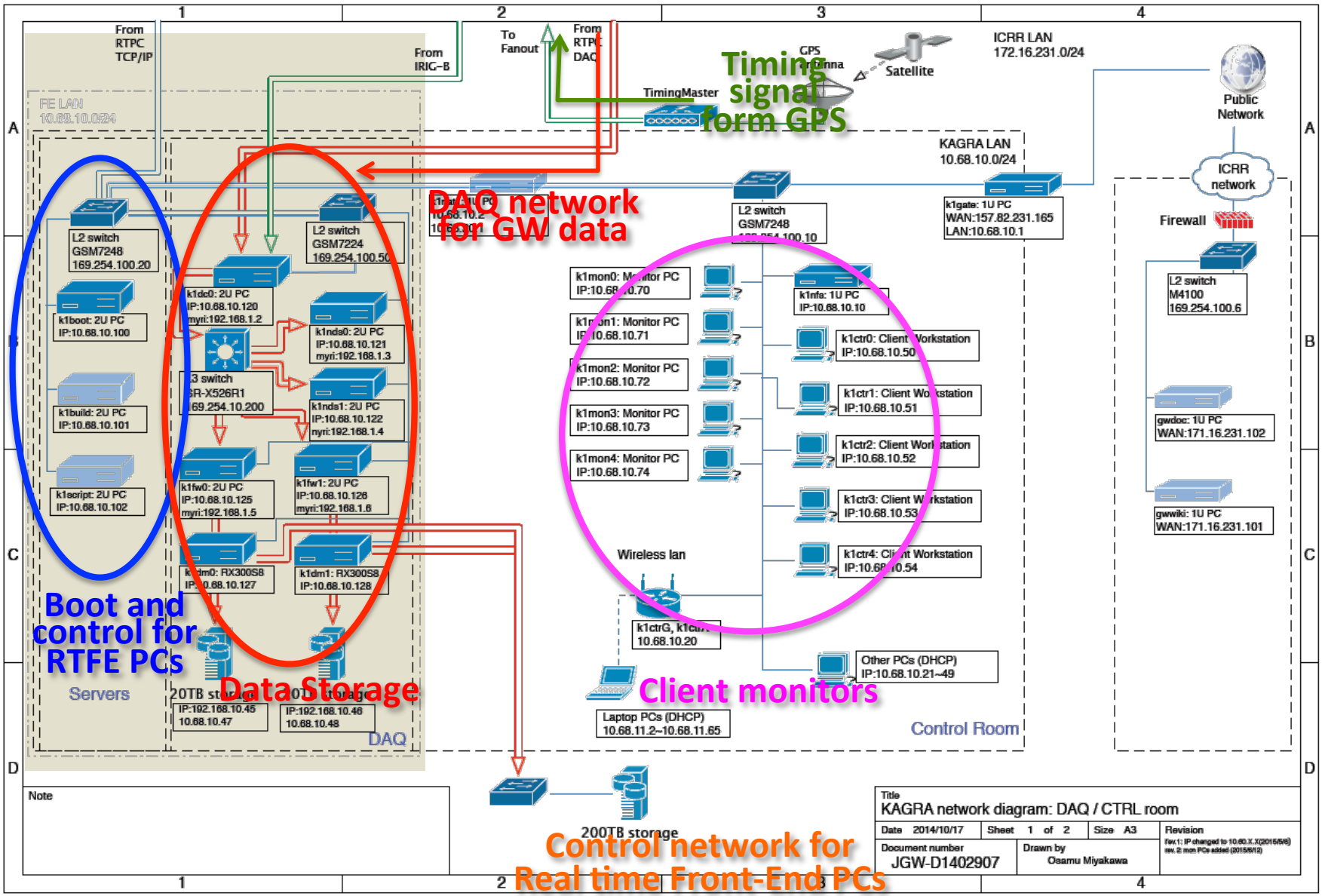
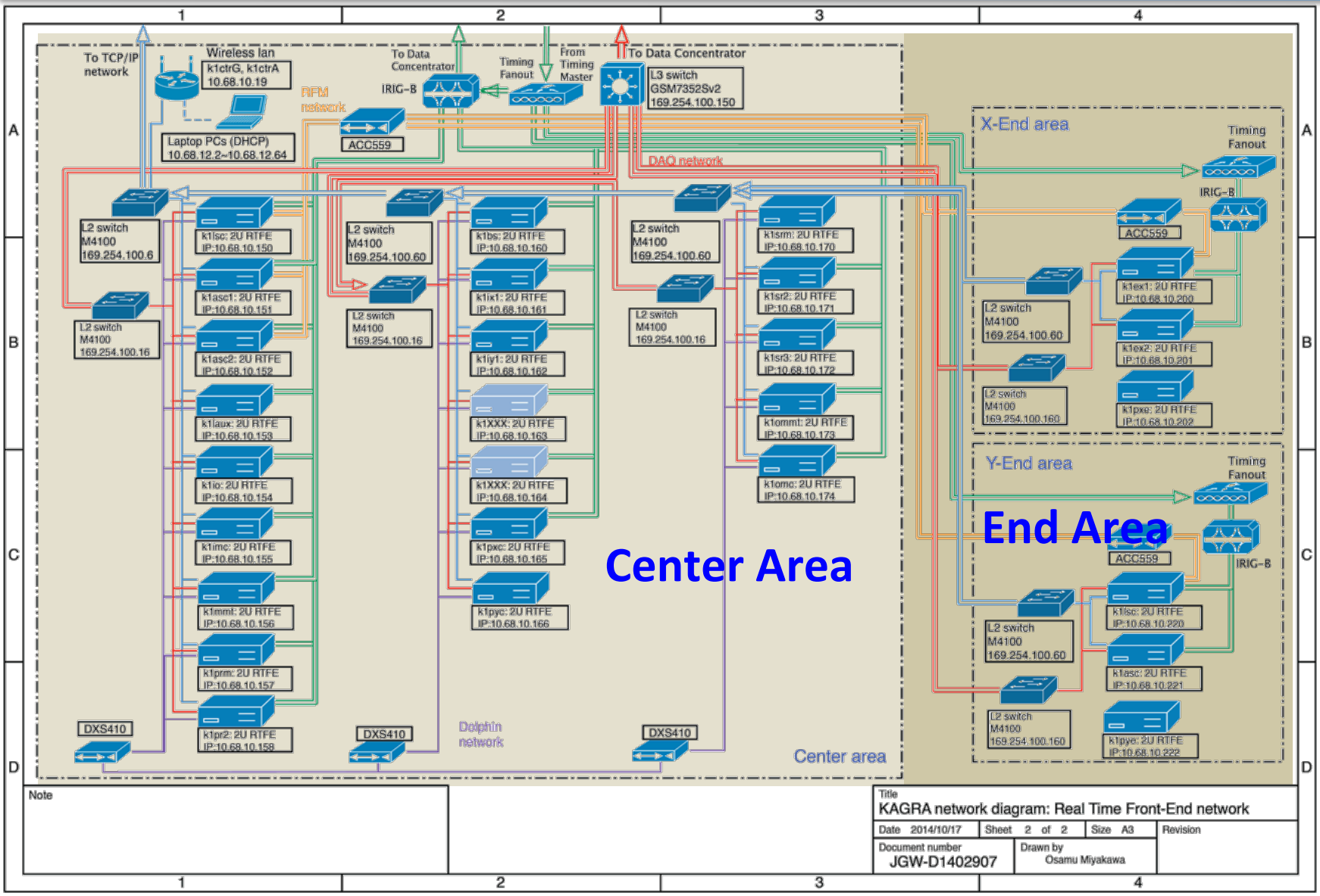
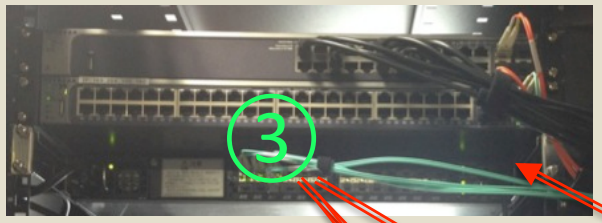


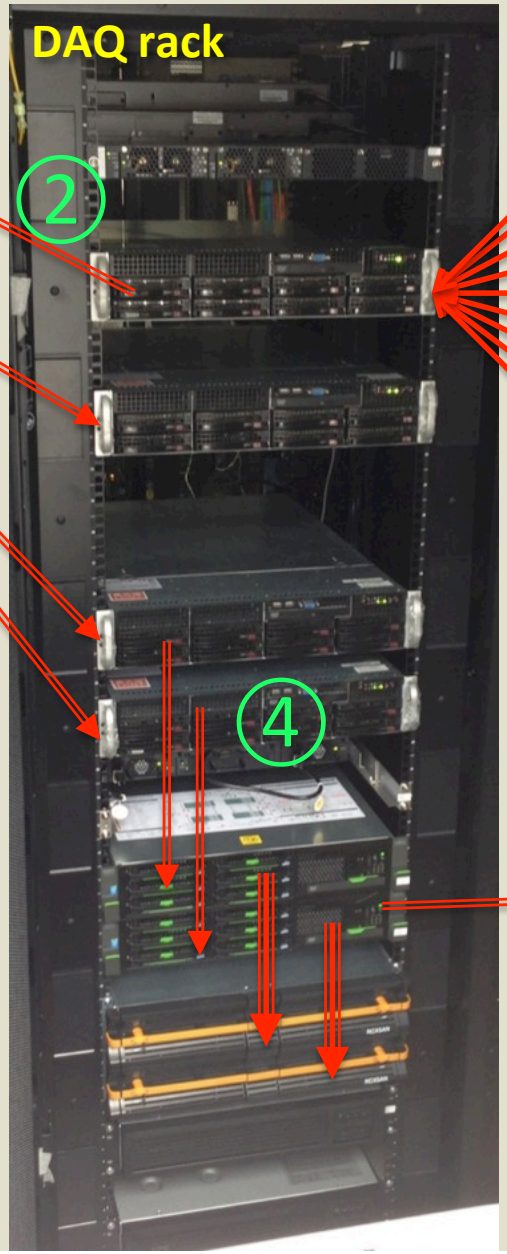
Diagram of KAGRA controls system for Real Time Front-End

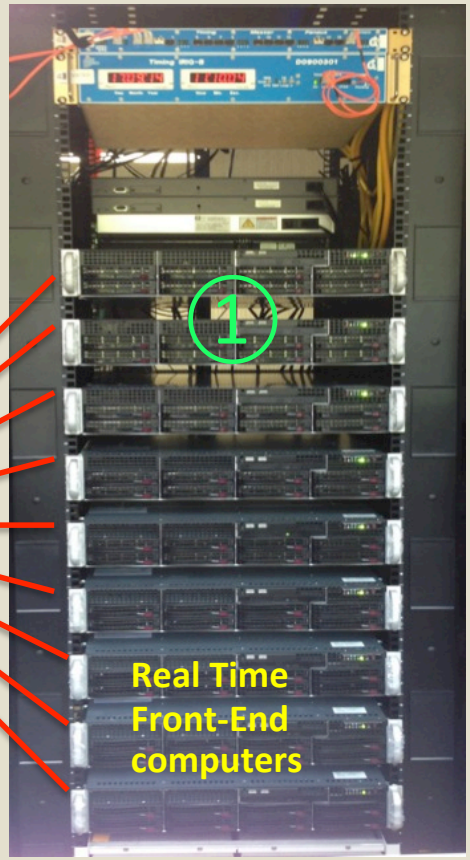


Control/DAQ network



Fujitsu: SR-X526R1
10GB low latency
switch





k1dc0

k1nds0

k1fw0

k1fw1

k1dm0
k1dm1

20TB storage
20TB storage

UPS

- **k1dc0**: data concentrator from all RTFE
- **k1nds0/k1nds1**: network data system as response server for realtime/past data request
- **k1fw0/k1fw1**: frame writer
- **k1dm0/k1dm1**: frame data manager for local 20TB storages and remote 200TB storage

Mine

Outside

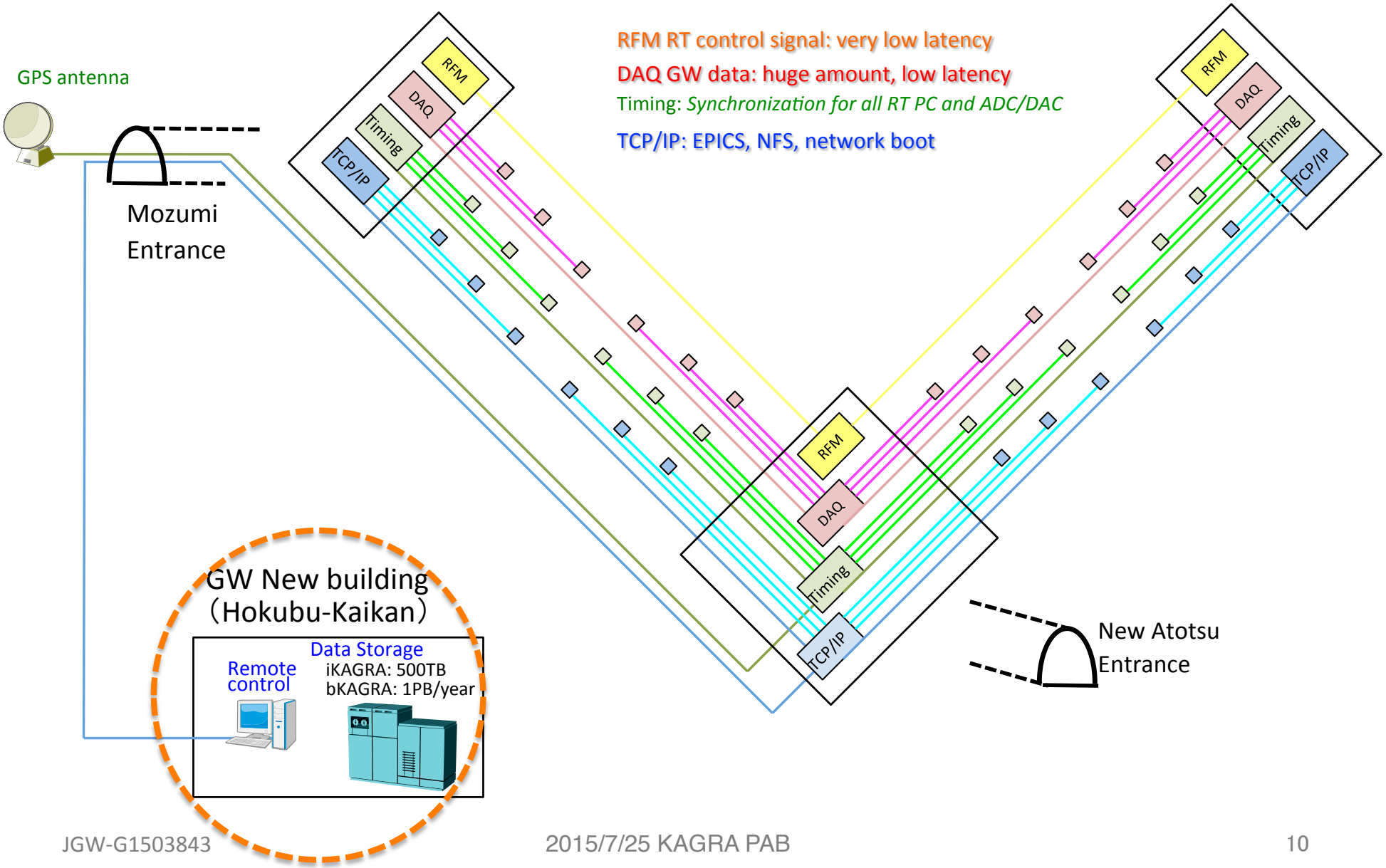
200TB
storage

Field rack

- A Field rack includes
  - IO chassis with ADC/DAC
  - AA/AI filter chassis
  - whintieng filter chassis
  - electronic circuit chassis
  - no Real time PCs
  - no DC power supplies

- Field racks are located in the laboratory area with a plastic cover to avoid humidity by heating of electronics
  - inside temp. : 25~30℃
  - inside humidity: 45~35%
  - outside humidity: 70~90%

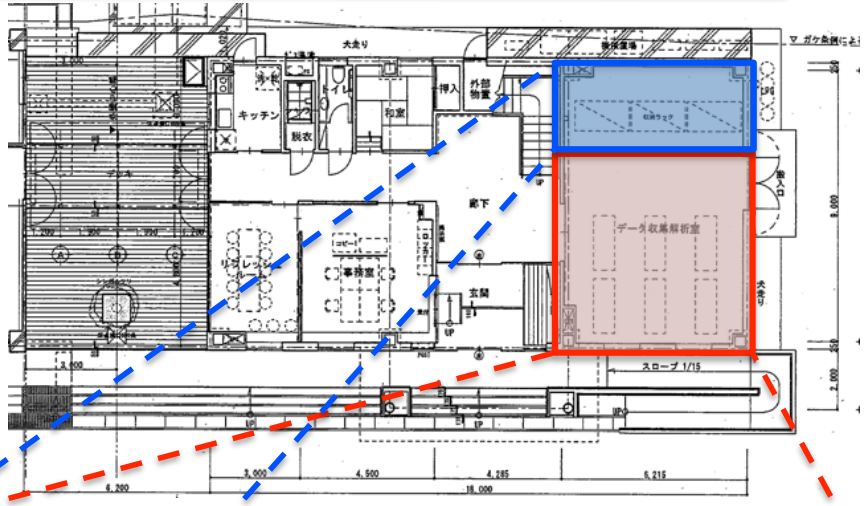
Network design

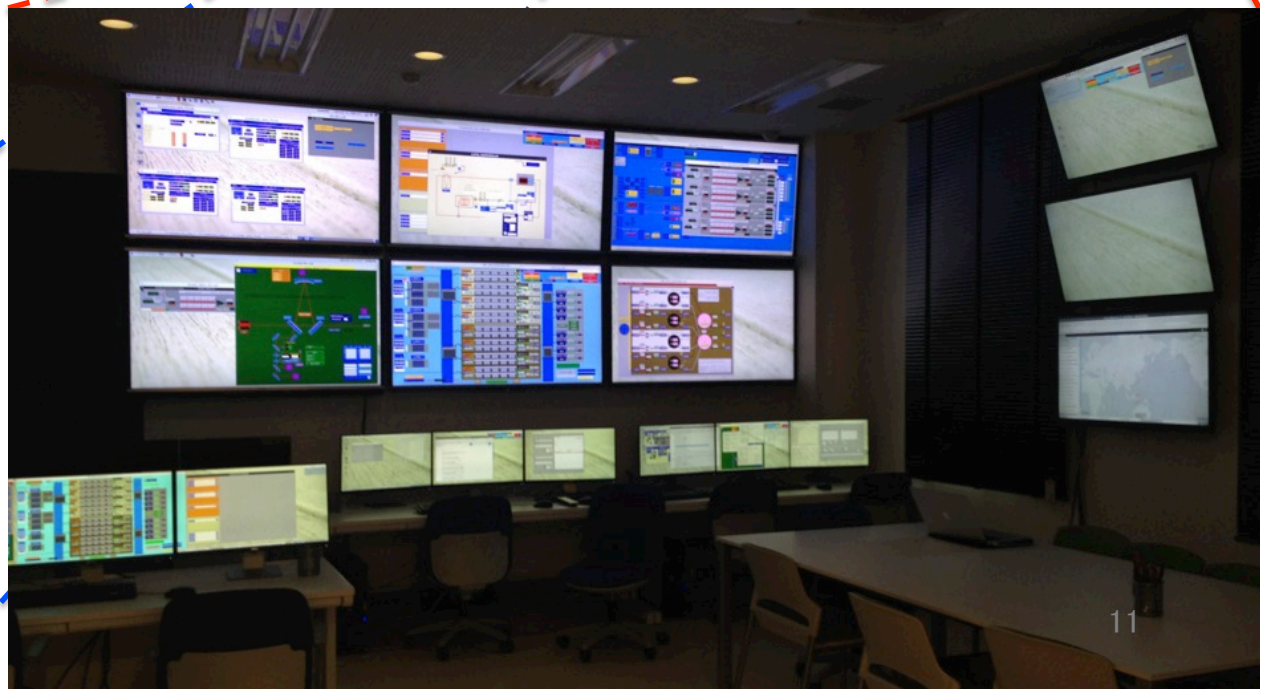


Remote control room

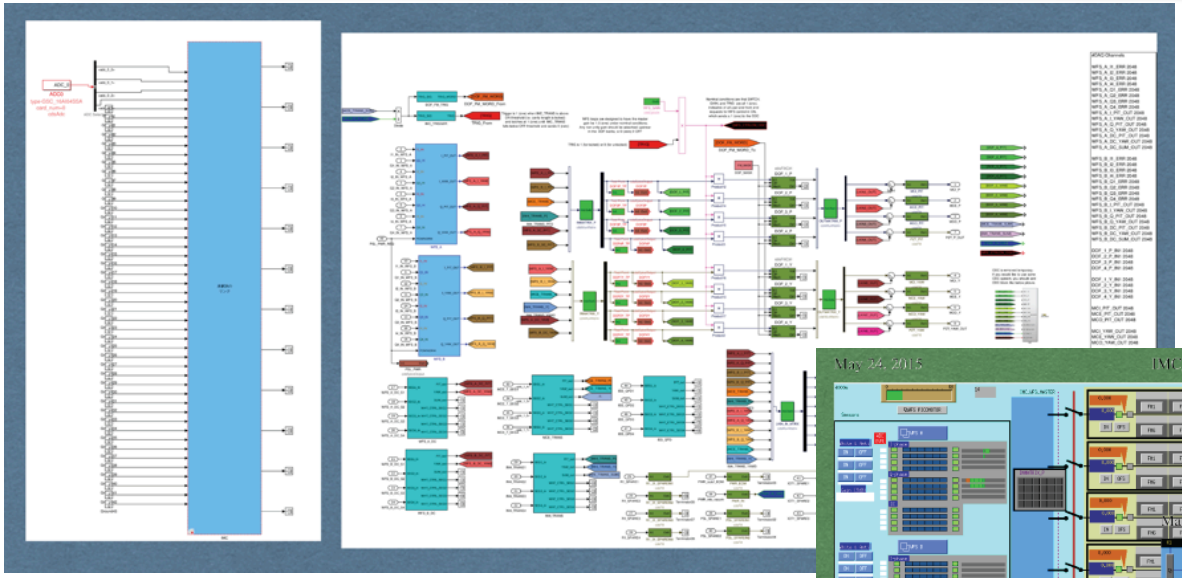
- 5 desks with 3 monitors
- 7 large monitors for sensitivity etc.
- 3 middle monitors for detailed information.
- 7 small monitors for beam spots.

- 200TB storage in the small server room.

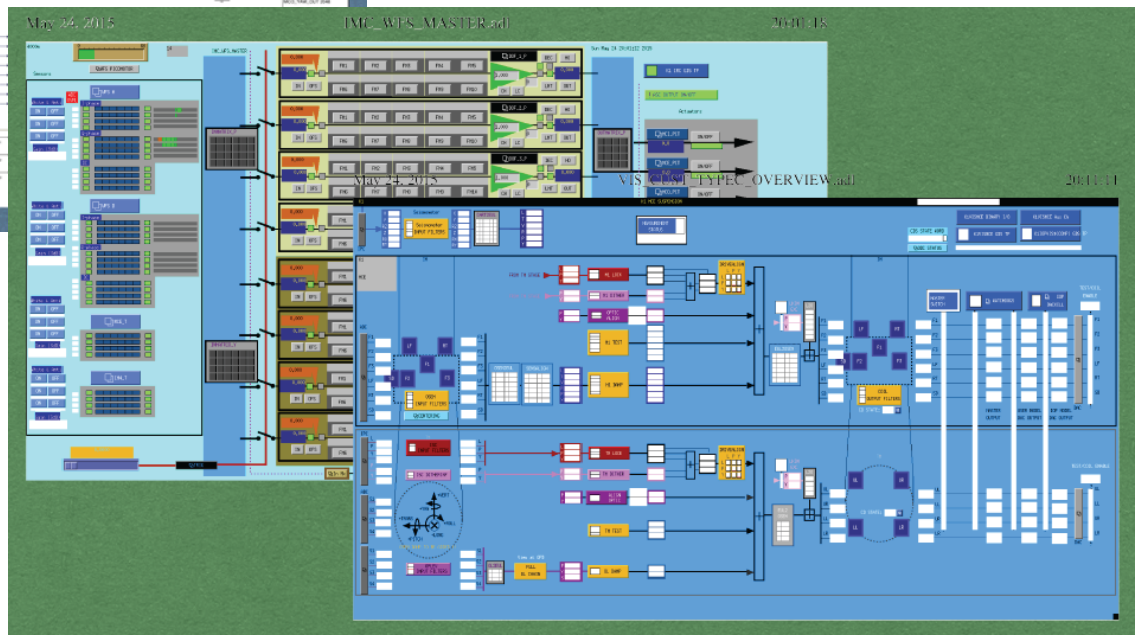




RT models, MEDM screens



- ADC/DAC channel are assigned here.
- Built on Matlab, Simlink



- MEDM on EPICS as a human interface

- **Initial models are being developed by DGS referring to LIGO models.**
  PSL, MC SUS, ASC, LSC
- **VIS group are developing a model for Type B suspension.**

To do

- Real time models and MEDM screens for all subsystems
  - Basically this task should be assigned to each subsystem, but DGS may provide a typical initial model and screens.
- Installing Gurdian (script, diagnostic manager).
- 3km connection and delay test.

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AEL (Analog Electronics)

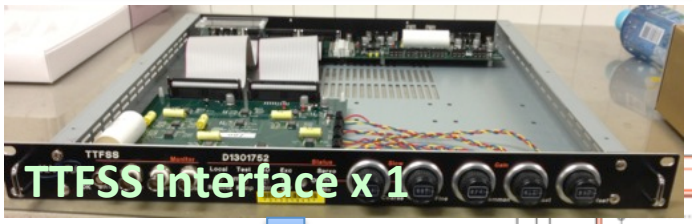
- Manufacturing almost of electronics for KAGAR
- Basically design is provided by each subgroup, but AEL may propose some appropriate designs .
  - Using LIGO design as possible.
- Expected number of circuits: 150 kinds of item, 800 boxes!
  - May increase x1.5 times if actual drivers or interfaces are considered.
  - Prototype: 95 boxes, iKAGRA: 456 boxes, bKAGRA: 253 boxes

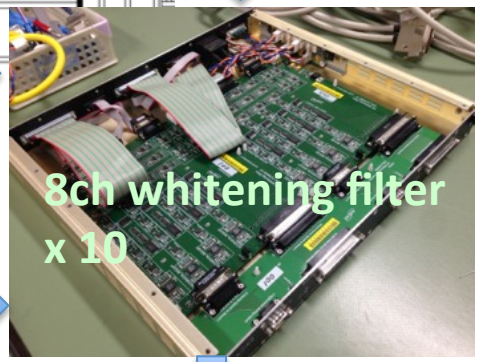
- Very serious problem: human resource
  - Osamu Miyakawa
    Chief, contact to subsystem for design and concept
  - Masahiro Kamiizumi
    Sub chief, Drawing diagram and board, Parts ordering, Assembling
  - Kyosuke Awai
    Joined from this February, working at other place during June to October.
- Started asking outside company from ordering parts, but still tasks are too many.

Assigned tasks in FY2015

Current task	Sub system	Qty.	achievement	status
LVDT driver	VIS	20	100%	Completed
LVDT distributor	VIS	20	100%	Completed
High power coil driver	VIS	6	80%	Being assembled to chassis
Low power coil driver	VIS	20	80%	Being assembled to chassis
Satellite box	VIS	10	90%	Being assembled to chassis, partially completed and being tested.
Satellite box	VIS	20	0%	Not started.
MC servo	IOO	1	90%	Being assembled and tested
RF PD	MIF	30	40%	Ordered to company, being manufactured
RF QPD	MIF	5	40%	Ready to be manufactured
RF PD interface	MIF	5	20%	Being Designed
RF QPD interface	MIF	5	20%	Being Designed
I&Q demodulator	MIF	5	100%	Completed
Whitening filter	MIF/GIF/DGS	10	100%	Done, being inspected
24V DC power strip	AEL	30	60%	Being manufactured

Manufactured electronic circuits for control





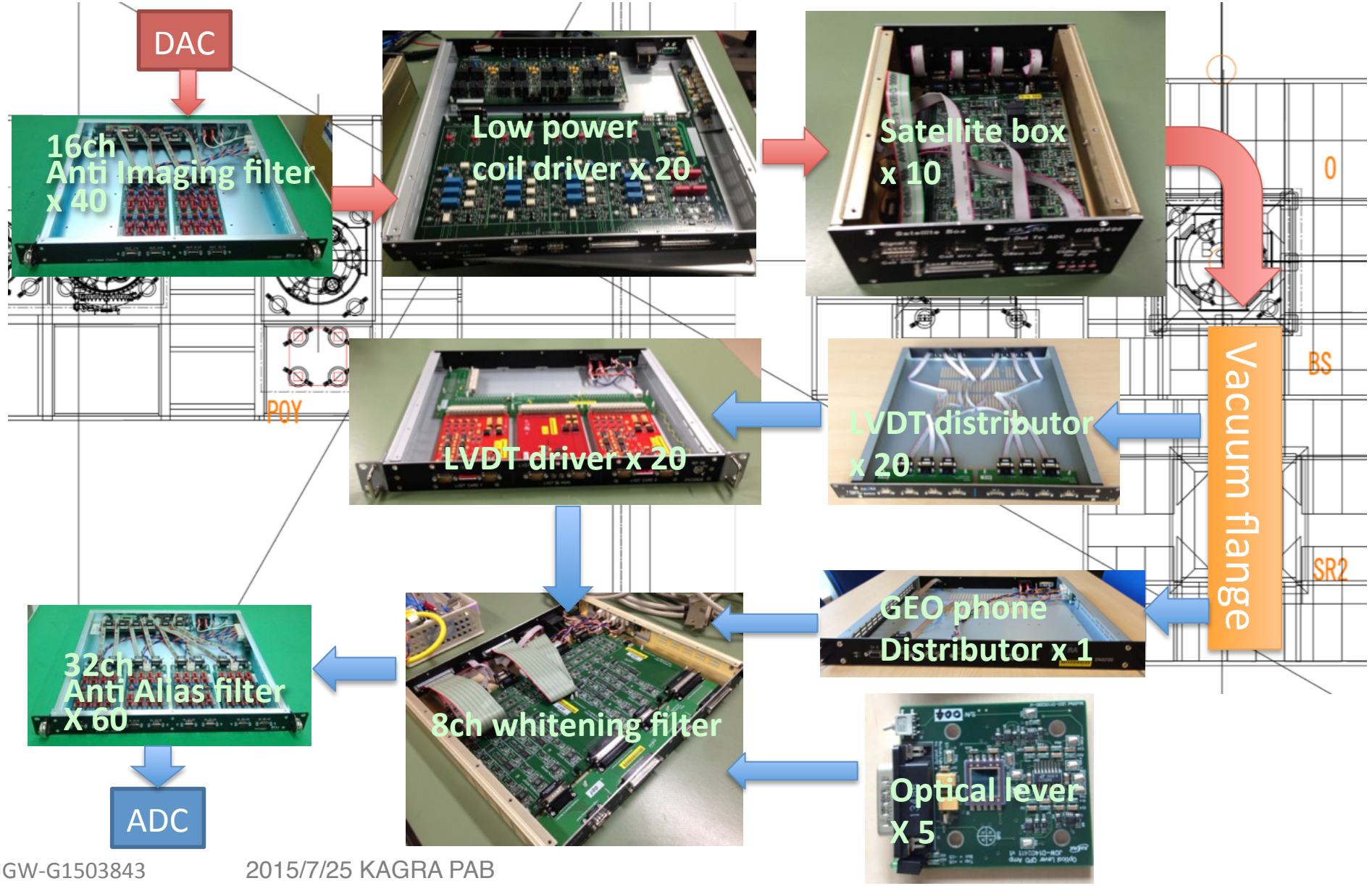
FSS

MC

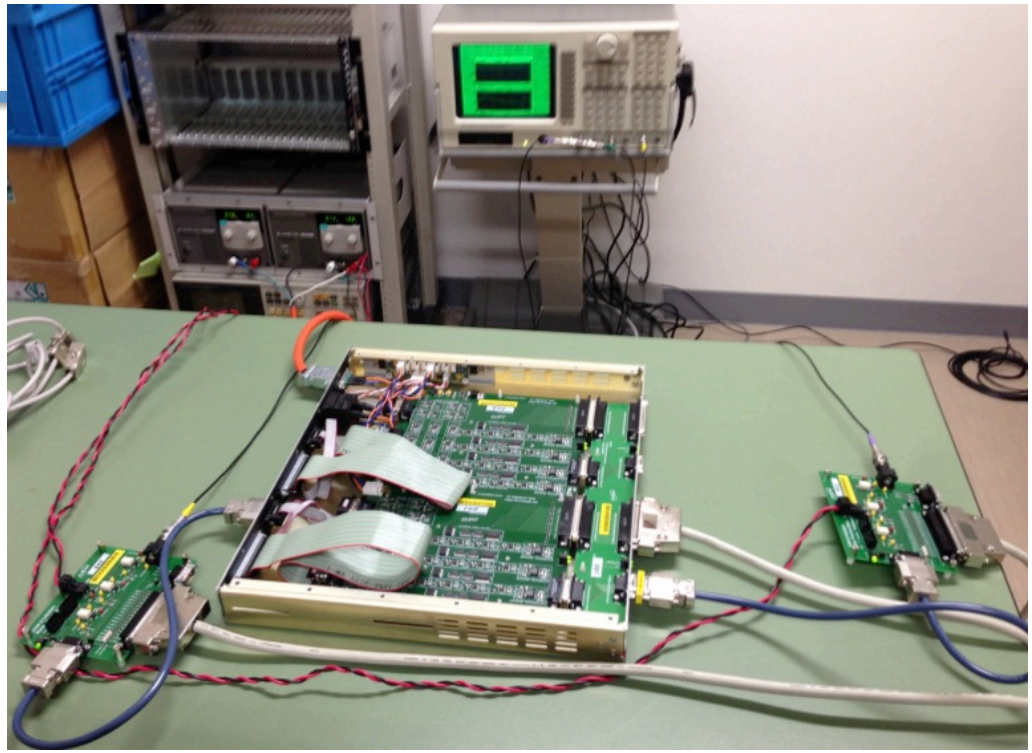
REFL

ADC

Manufactured electronic circuits for suspensions



Inspection



Whitening filter:

- 4bit for 0-45dB variable gain, 3dB step
- 3bit for 3 orders whitening with 1Hz zero: 10Hz pole
- 8ch in 1U chassis

Test for whitening filter:

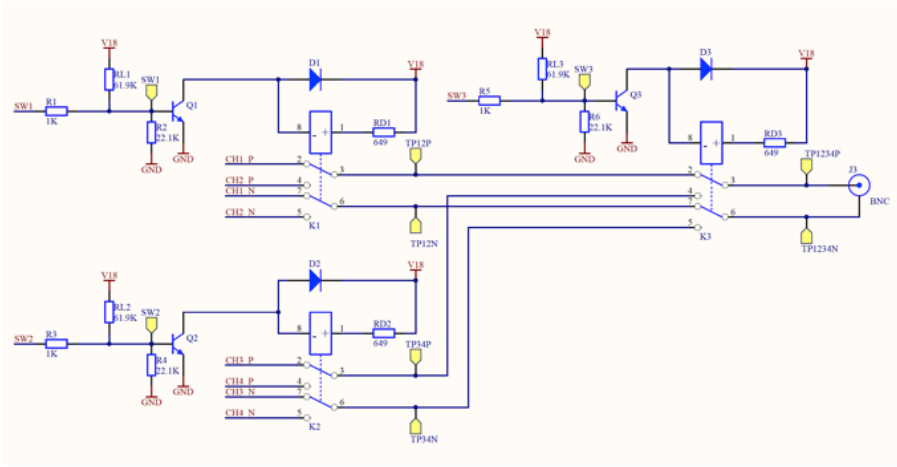
T.F. : 8ch x (4x4)bit x 3bit = 384

Noise: 8ch x (4x4)bit x 3bit x 4span = 1536

Total: 1920 measurements!

Automated inspection:

- Measurement using a SR785 controlled by python code on a remote computer through GPIB.
- Remote controlled relay switch box to measure D-SUB 9pin 4ch signals at once using a single channel SR785.



Summary

DGS:

- Quite going well.
- Real time models and MEDM screens should be prepared.

AEL:

- We are continuously manufacturing analog circuits, but human resource is a very serious issue.