Modification Plan for Common Mode Servo Board

Yuta Michimura

Ando Group

Department of Physics, University of Tokyo

aLIGO One

- LIGO-D0901781 (assembly)
- LIGO-D040180 (schematic)
- LIGO-D0901784 (schematic of interface board)
- LIGO-D0901846 (schematic of low noise power module)
- boards are modified for each servo (IMC, ALS, CARM)

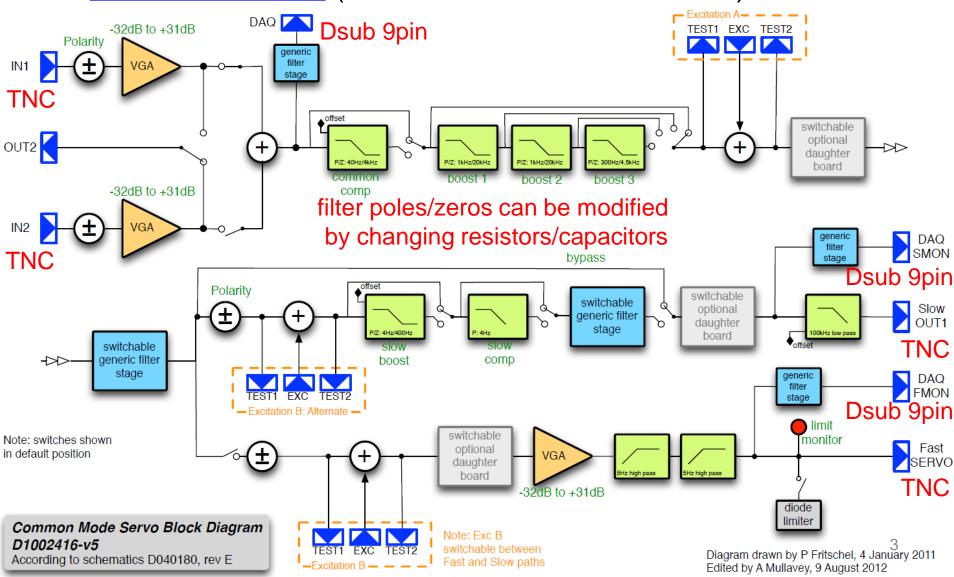
LIGO-E1200177, awiki (modification summary)



rear panel

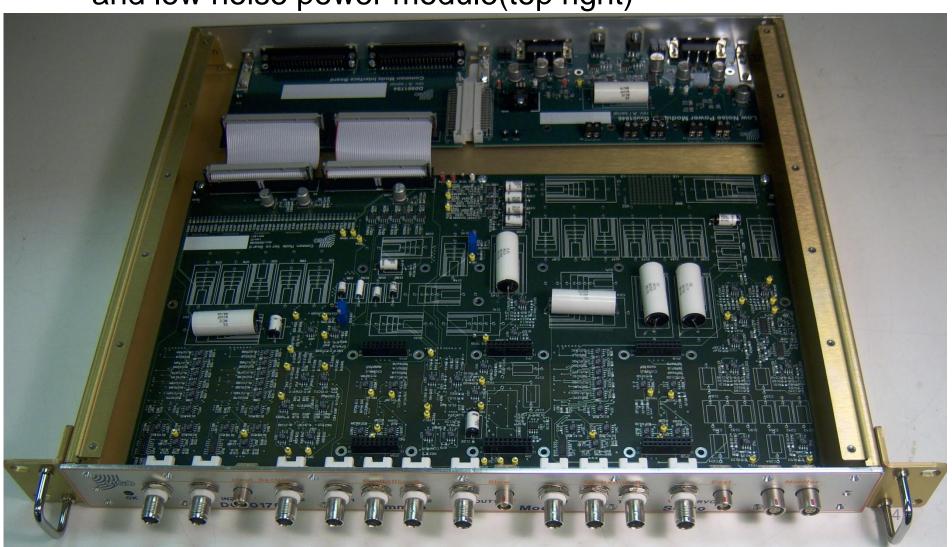
Block Diagram

LIGO-D1002416 (we also want to make rev E)



Inside

 consist from main board(bottom), interface board(top left), and low noise power module(top right)

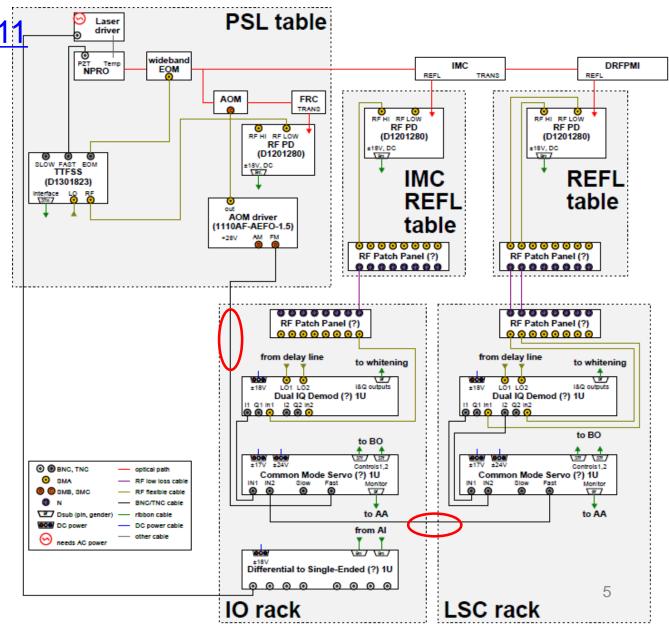


aLIGO Usage Example

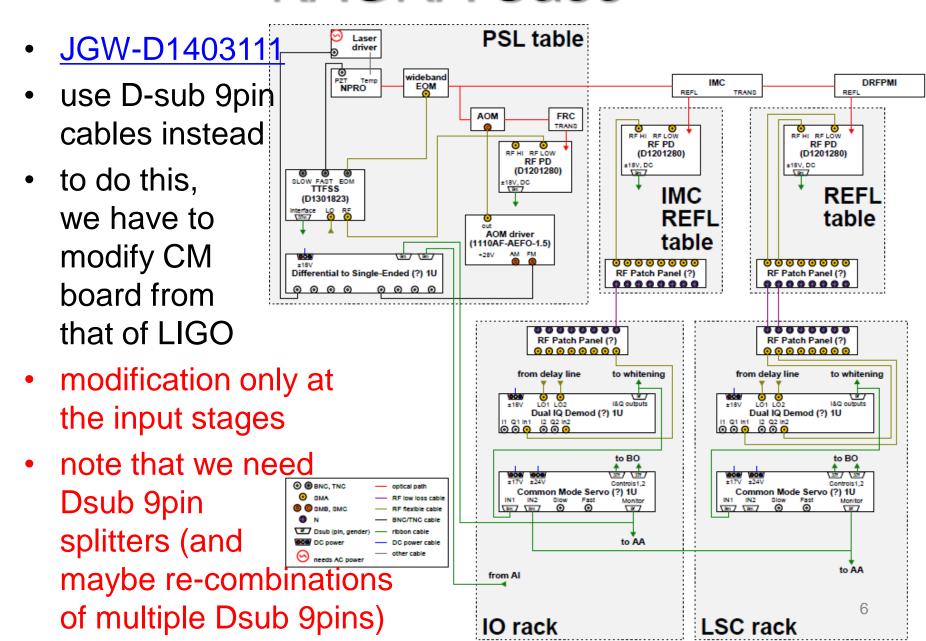
JGW-D1403111

 long line single-ended cables

maybe we want to avoid these for eliminating ground loops



KAGRA Case



Inputs and Outputs

- Inputs
 - CM Board for IMC

IN1: IMC REFL (from Dual IQ Demod Dsub 9pin)

IN2: additive offset (from CARM CM Board Dsub 9pin)

- CM Board for CARM

IN1: REFL/ALS common (from Dual IQ Demod Dsub 9pin)

Detected RF Level

IN2: REFLVAC (from Dual IQ Demod Dsub 9pin)

• Outputs

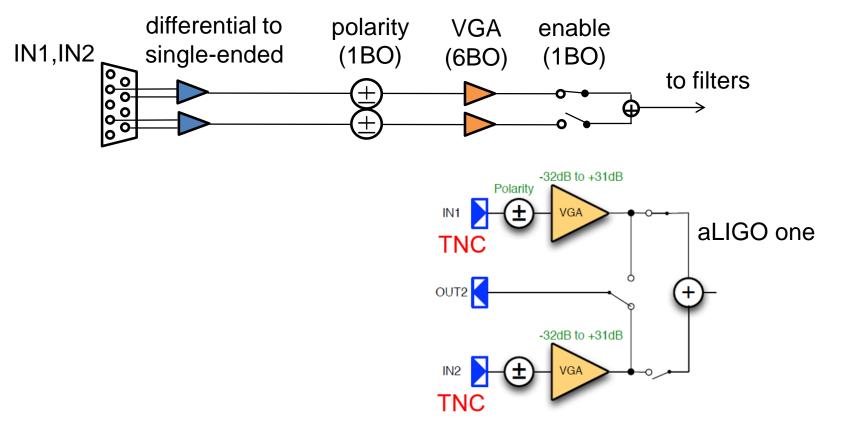
INmon, Fast, Slow in Dsub 9pin

MON P 1 100n P 2 PMON N 7 SMON N 8 Dsub 9pin from IQ Detected Io Level

BY Demodulated I-Phase Output

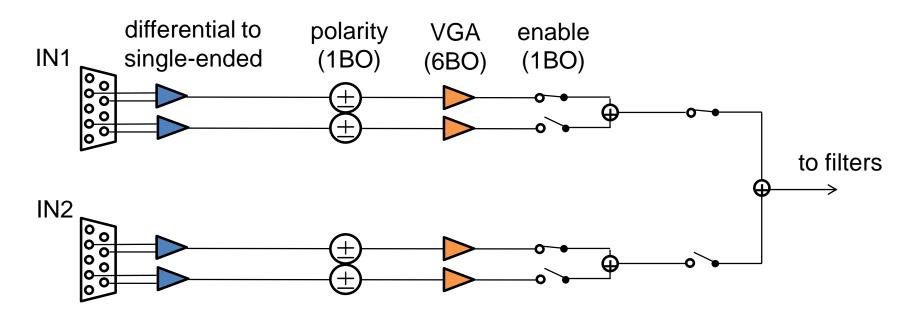
Possible Modification 1

- 1 Dsub 9pin inputs, gain for each
- many Dsub re-combinations
- possibly sum board with VGA is needed (aLIGO has CM Sum Board <u>LIGO-D1200148</u>)



Possible Modification 2

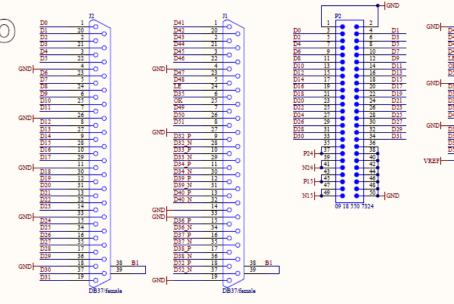
- 2 Dsub 9pin inputs, gain for each
- less Dsub re-combinations outside the CM board
- we need extra 16 BO channels
 - → extra Dsub 37pin needed



Binary Outputs

• <u>LIGO-D0901784</u>

 basically, already full



```
Digital Inputs:
D[ 5.. 0]: Gain slider input 1
D[11.. 6]: Gain slider input 2
         : Input 1 enable
         : Input 2 enable
         : Output 1 switch
D[16..15]: Number of boost stages
         : Compensation enable
         : Excitation A enable
         : Option A enable
         : Polarity slow path
         : Common filter enable
         : Fast path enable
         : Fast path polarity
         : Slow path option enable
         : Bypass enable
         : Slow output offset +5V fixed
         : Slow output offset enable
         : Slow path compensation enable
         : Slow path boost enable
         : Slow path filter enable
         : Fast path limiter enable
D[46..41]: Gain slider fast path
         : Excitation B enable
         : Option B enable
D[49]
         : Excitation slow path
         : Polarity input 1
         : Polarity input 2
         : Latch enable
```

```
: Fast path limits reached
         : Voltages are within range
Analog Inputs:
         : Common path offset adjust
         : Slow path offset adjust
         : Slow path output offset
         : Input monitor
D[33
         : Monitor at split
D[34]
         : Fast monitor
D[39]
         : Slow path feedback monitor
D[40]
         : Slow monitor
Spares:
         : Not used
                                      10
```