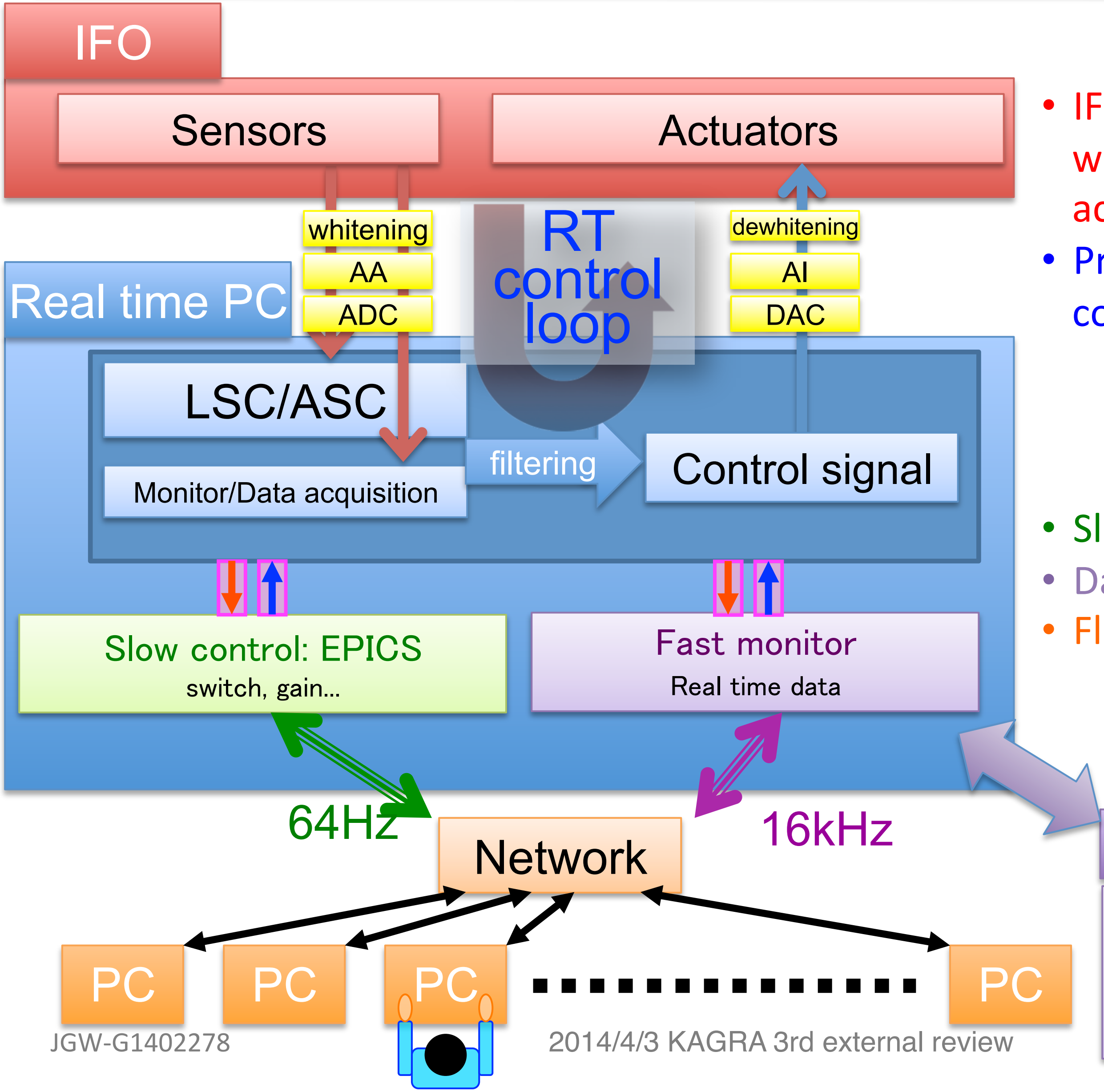
KAGRA 3rd External review for DiGital System subgroup

2014/4/3(Thu) @ICRR

Osamu Miyakawa

Concept of digital system



Data storage

16kHz full data
1 minute data
1 second data

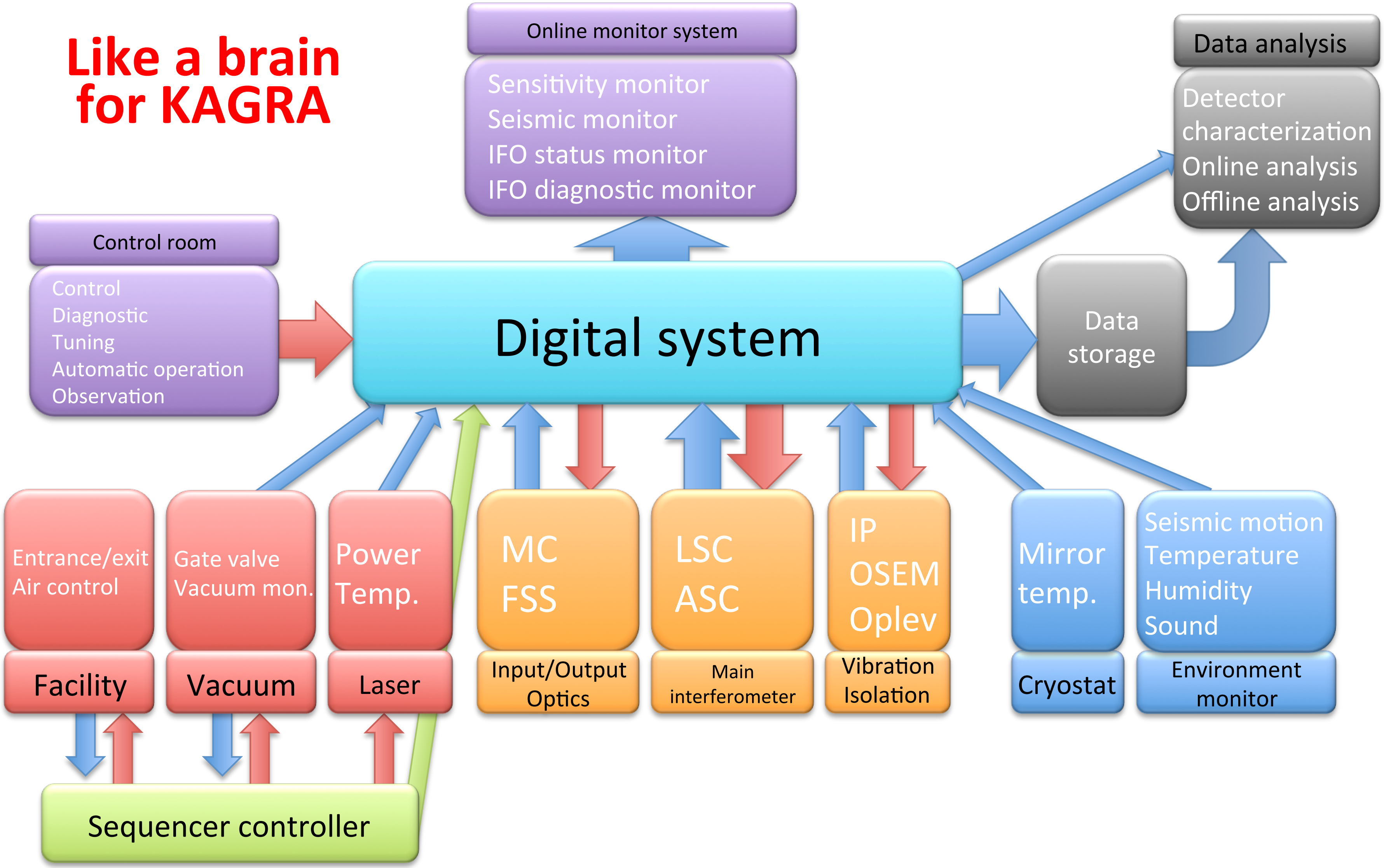
Real time control

- IFO is a multiple DOF plant which has many sensors and actuators
- Produces control signal using computers

Data access without breaking control

- Slow control by using EPICS
- Data acquisition(DAQ)
- Flexible human interface

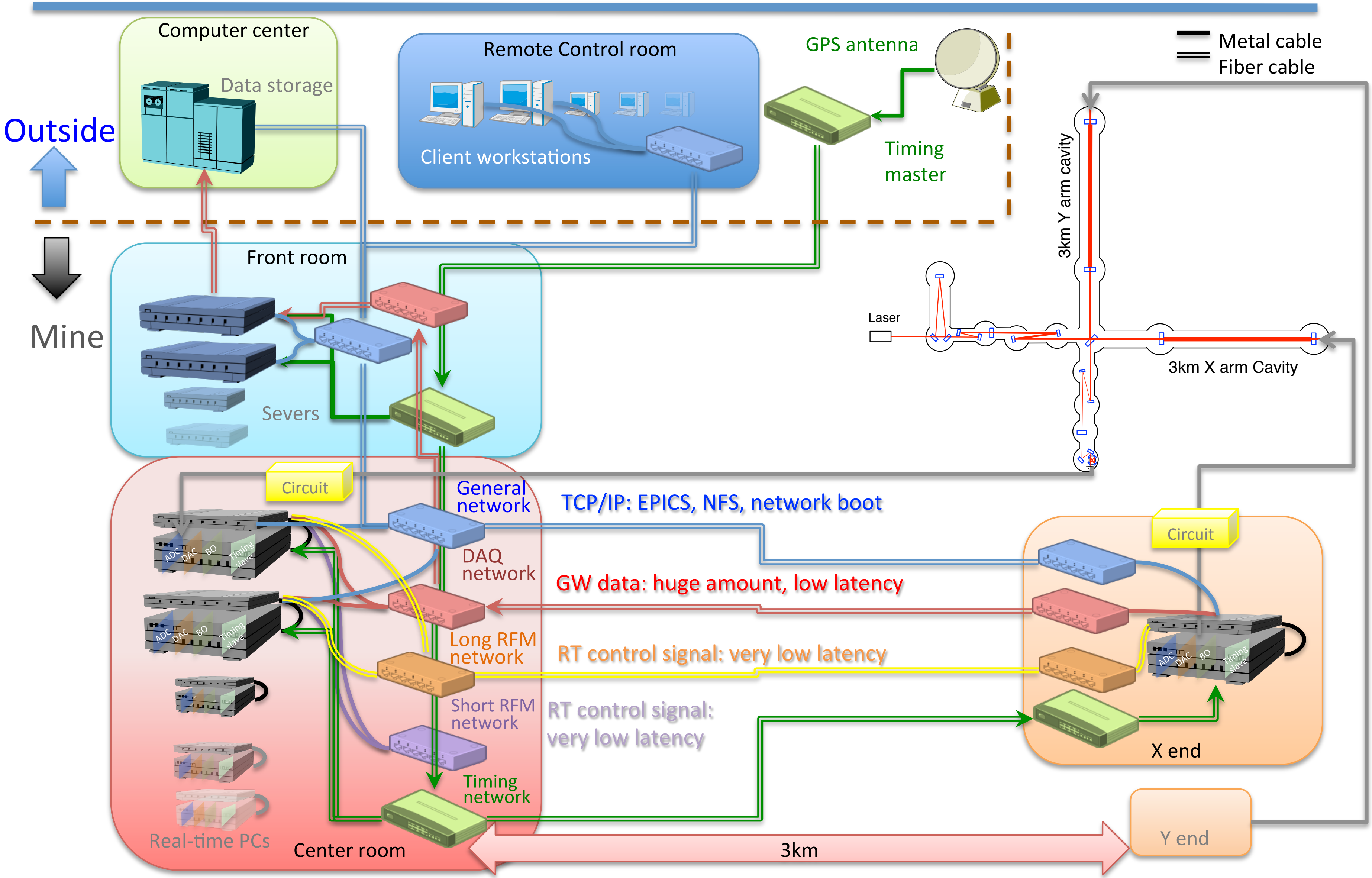
Important role as interface to subsystems



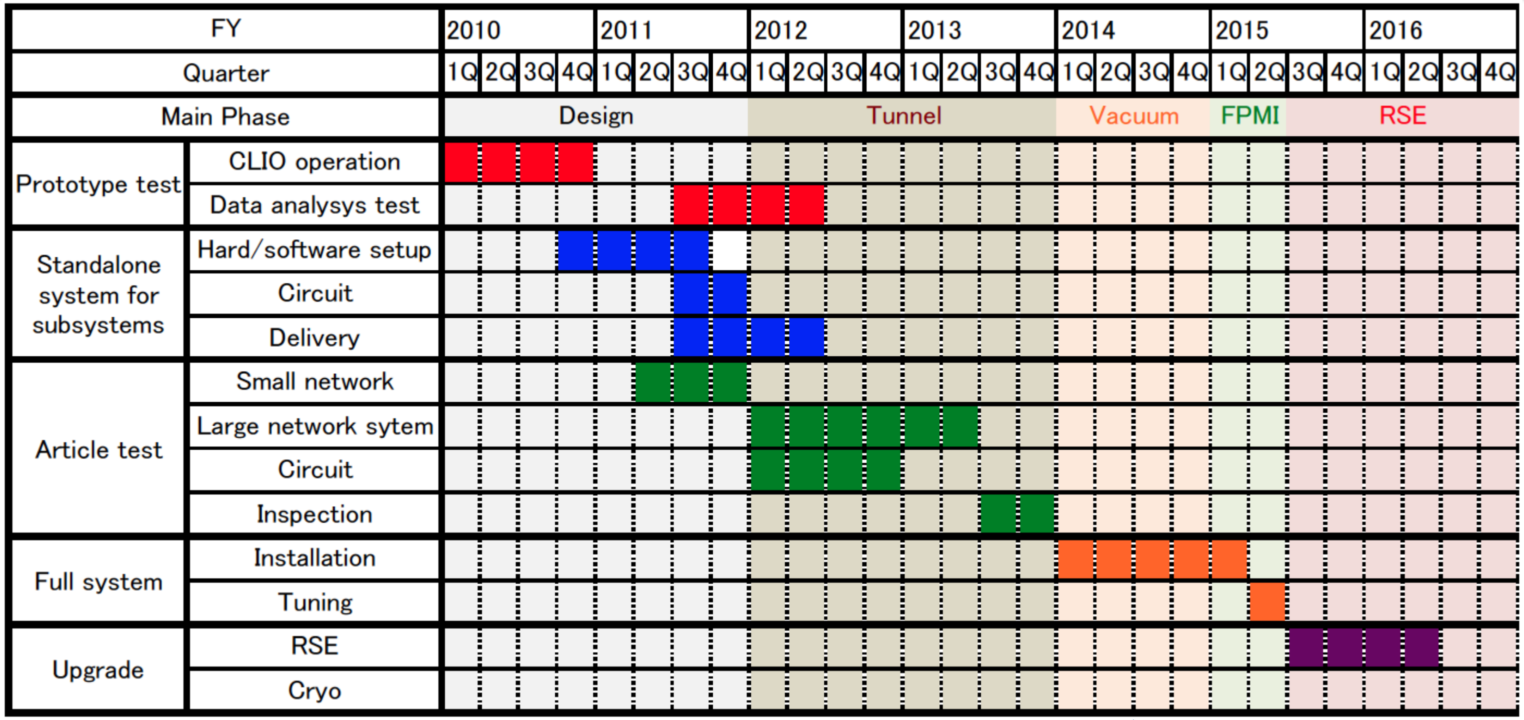
Objectives

1. Function as Real time control
   - For complicated multiple DOFs
2. Function as Data acquisition system for GW waves
   - Control signal = GW data
3. Function as IFO tuning system
   - Reducing time for improving sensitivity
4. Function as Automatic IFO operation
   - Stable observation
5. Function as information collecting system for IFO
   - Automatic channel assignment for huge number of channels

KAGRA control network design



Schedule



Installation into KAGRA mine

A. 2009-2010 prototype test @ CLIO (done)
   – Basic IFO operation and noise performance

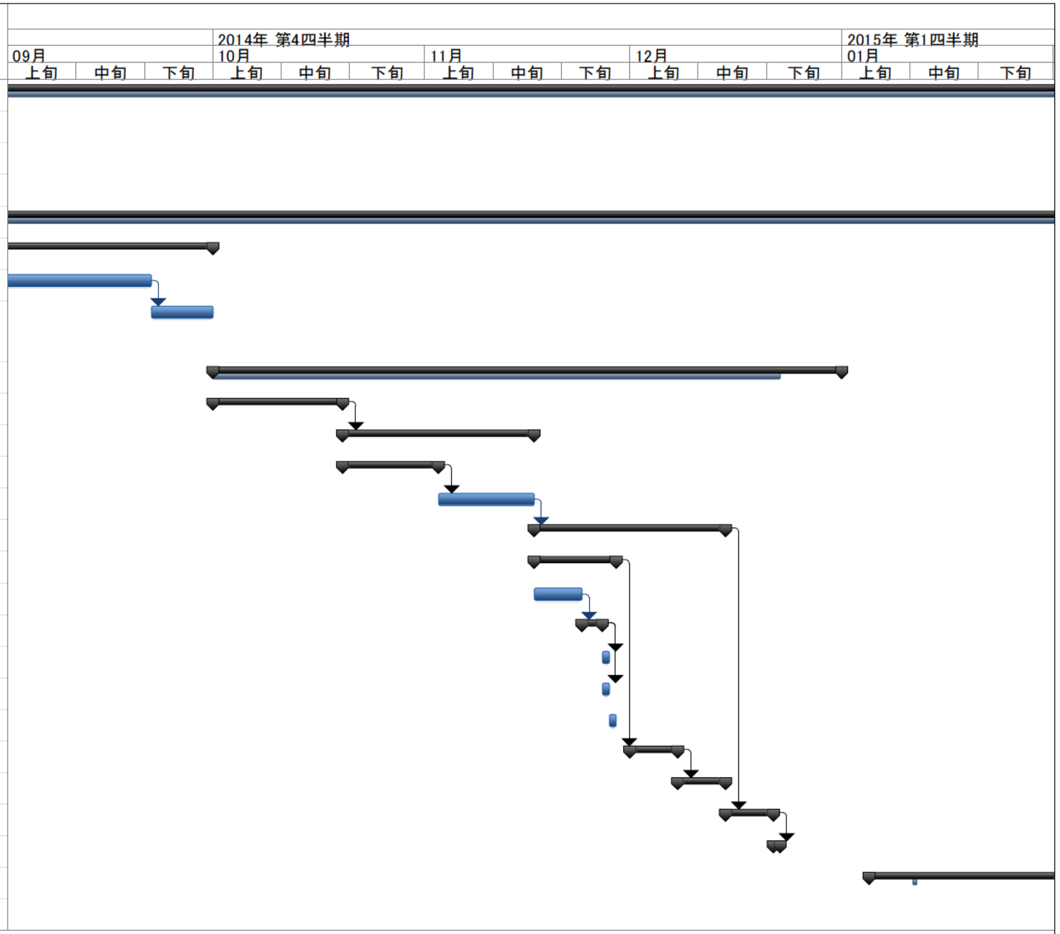
B. 2011~ standalone system for subsystem (done)
   – Data analysis, VIS, (IOO, CRY…)

C. 2011 Small network test with 1 master and 2 RT PCs (done)
   – GE RFM, Dolphin RFM, DAQ, timing network

D. 2012-2013 Full test@ Kamioka new building
   – Closer to real scale PCs and network

Schedule for installation of DGS full system

ID		タスク モード	タスク名	期間	開始日	終了日
1			**DGS**	**2404日?**	**2010/09/01**	**2017/03/31**
2	✓		Standalone system	578日?	2010/09/01	2012/03/31
3	✓		Small network system	731日	2011/04/01	2013/03/31
4			Large network system	730日	2012/04/01	2014/03/31
5			**Full system**	**365日**	**2014/04/01**	**2015/03/31**
6			**Assembling**	**183日?**	**2014/04/01**	**2014/09/30**
7			Test using LNS	174日?	2014/04/01	2014/09/21
8			Release from existing rack	9日?	2014/09/22	2014/09/30
9			**Installation**	**92日**	**2014/10/01**	**2014/12/31**
10			**Rack**	**19日?**	**2014/10/01**	**2014/10/19**
13			**Computers**	**28日?**	**2014/10/20**	**2014/11/16**
14			**Servers**	**14日**	**2014/10/20**	**2014/11/02**
23			RT front-end	14日?	2014/11/03	2014/11/16
24			**Network**	**28日?**	**2014/11/17**	**2014/12/14**
25			**Center area**	**12日?**	**2014/11/17**	**2014/11/28**
26			TCP/IP	7日?	2014/11/17	2014/11/23
27			**DAQ**	**3日?**	**2014/11/24**	**2014/11/26**
30			RFM	1日?	2014/11/27	2014/11/27
31			Dolphin	1日?	2014/11/27	2014/11/27
32			timing	1日?	2014/11/28	2014/11/28
33			**X arm**	**7日?**	**2014/12/01**	**2014/12/07**
39			**Y arm**	**7日?**	**2014/12/08**	**2014/12/14**
45			**Timing**	**7日?**	**2014/12/15**	**2014/12/21**
52			**Front room**	**1日?**	**2014/12/22**	**2014/12/22**
54			**Control room**	**28日**	**2015/01/05**	**2015/02/01**
56			Upgrade to RSE	365日	2016/04/01	2017/03/31



- Full system installation: 2014/10-2014/12
- Connection to subsystems: 2015/1~

Schedule

DGS controls and DAQ system will be installed in 2014.10 into mine.

VIS for iKAGRA
- Type-B: 1 for BS (in 2014.12)
- Type-Bp: 6 for PR2, PR3, IXA, IYA, EXA, EYA (in 2014.9)
- Type-C: 1 for MCF, MCE, IFI, IMM (in 2014.7)

for bKAGRA
- Type-A: 2 for EXV, EYV (in 2015.3)
- Type-A: 2 IXV, IYV (in 2015.9)
- Movement from IXA, IYA, EXA, EYA to PRM, SRM, SR2, SR3 (in 2015.9)

AOS: End: for BRT control (in 2016.1, or 2014.10 for test)

MIF for LSC: REFL, AS_RF, AS_DC, POP, POX, POY (around BS chamber in 2015.1)

End: TRX, TRY through RFM to LSC (in 2015.1) and ASC (in 2016.1)

ASC: REFL, AS_RF, POP (around BS chamber in 2016.1)

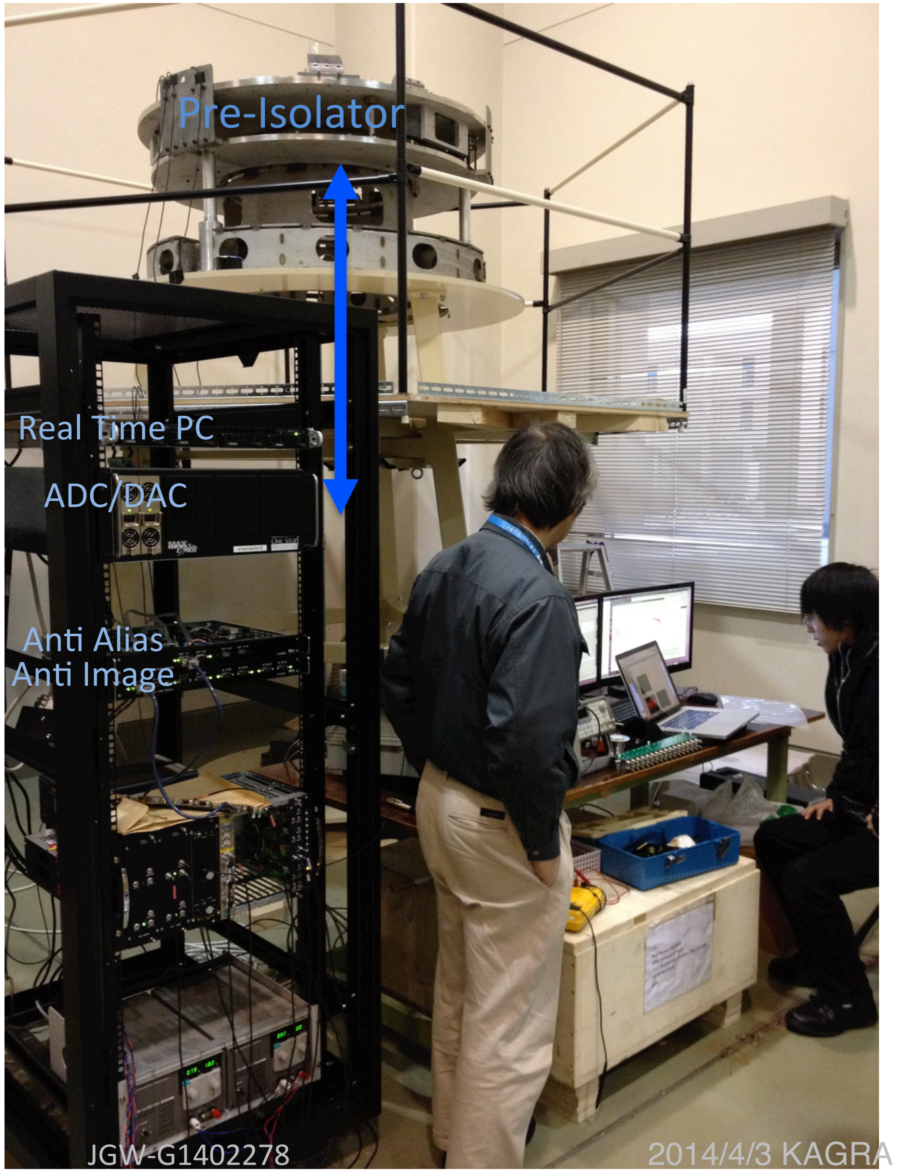
AUX: Green Lock or others from POP, POS through RFM to LSC (around BS chamber in 2016.1)

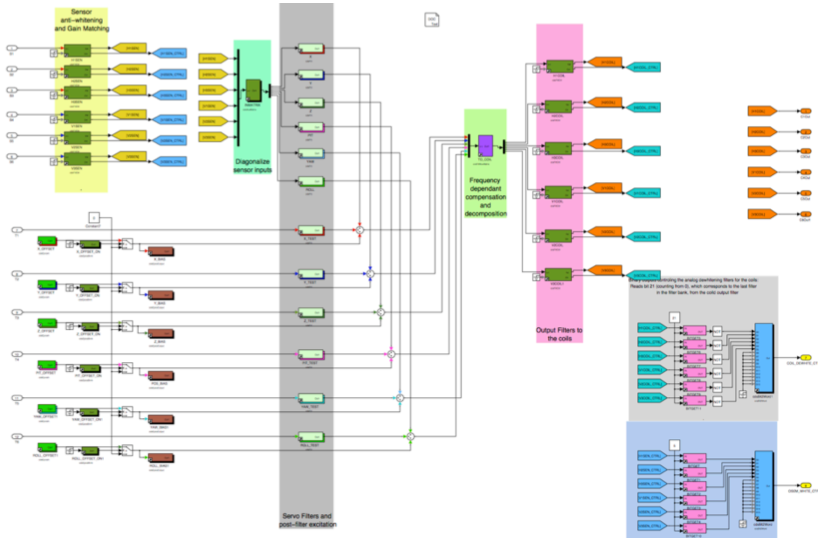
IOO: FSS thermal control, MC control (around MC chamber in 2014.10)

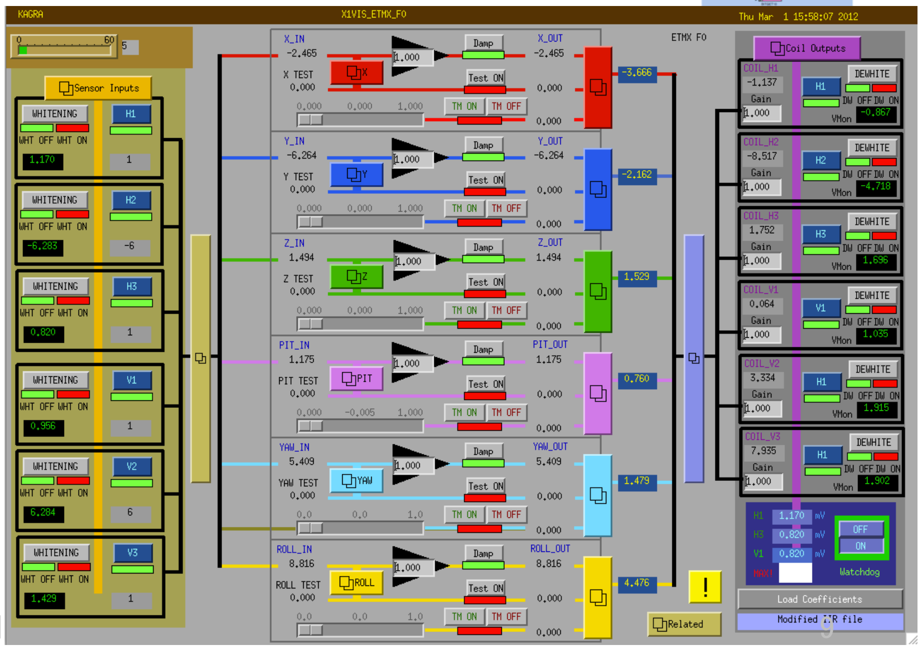
: Prototype test: at Kashiwa (in 2014.6)

GIF: for Seismometer at center of each arm (in 2014.10)

Digital control system for Pre-Isolator







Items for Real Time control

	Stand alone FY2010-	Small network FY2011	Large network FY2012, 2013	Full system FY2014~
Real time PC	1	2	5	~30
IO chassis	1	2	5	~30
ADC	1	2	~10	~65
DAC	1	1	~10	~45
Binary Output	1	0	~10	~85
Long distance RFM	0	1	2	3
Short distance RFM	0	1	2	2
DAQ network switch	0	1	4	4
Timing switch	0	1	3	3
Boot server	0	1	1	1
Network file system	0	0	1	1
system server	0	0	1	3
NAT	0	0	1	2
Data concentrator	0	0	1	1
NDS distributer	0	0	1	2 (redundant)
Frame writer	0	0	2 (redundant)	2 (redundant)
IRIG-B switch	0	0	1	3
Data storage	1TB (local)	1TB (local)	~20TB x2 (ext.)	~200TB (ext.)

Red: new items Green: increments

KAGRA

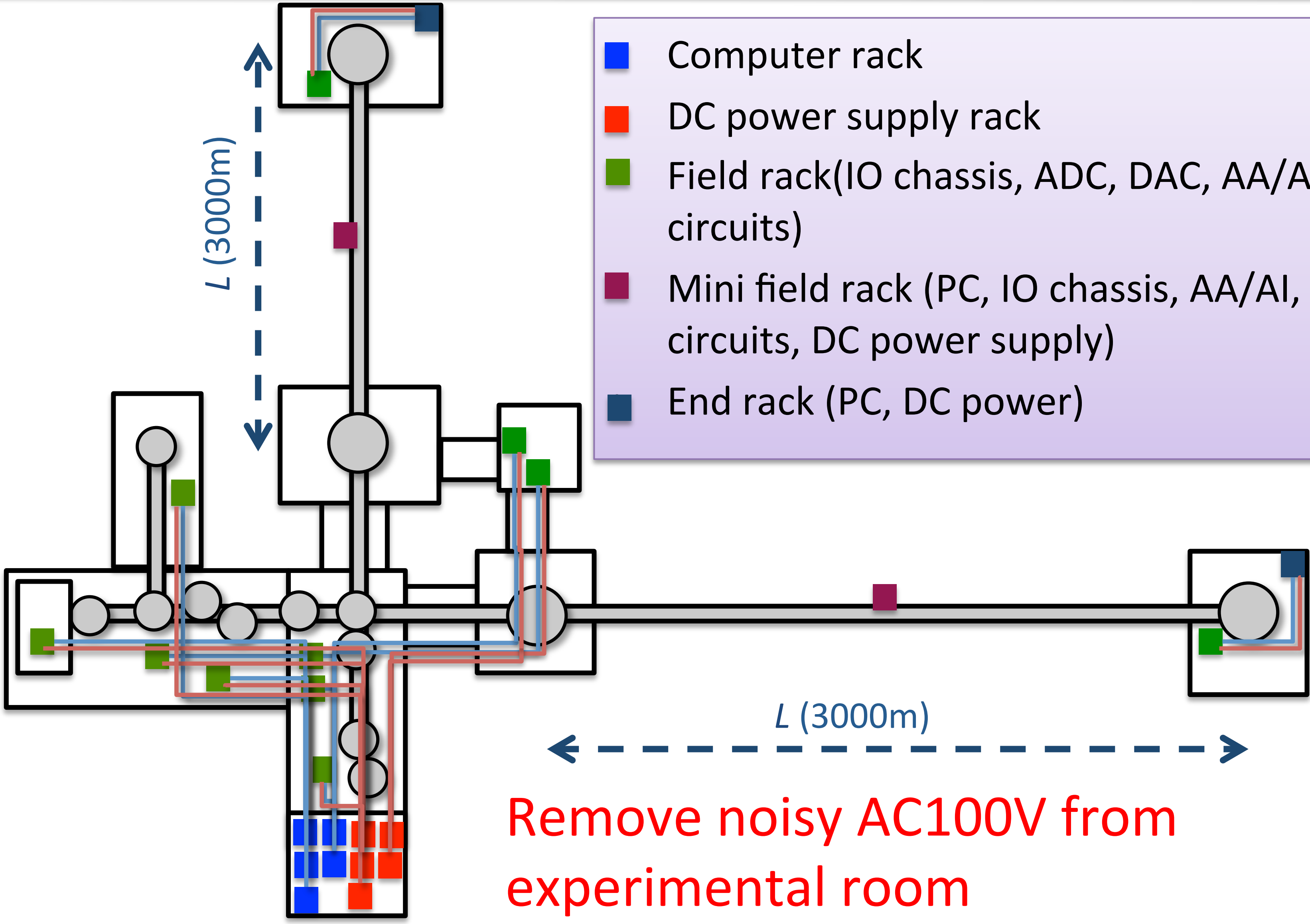
Number of PC/ADC/DAC/BO

RT PC Name	RT PC room	Roon No.	rack	IO chassi room	Room No.	Cable length	IO chassis Qt.	RFM	Dolphin	ADC	DAC	BO card	BO cards for wh.	BO cards for dewh.	Total cards	Items	Comments
k1io	C Control	1		FMC-Area	9	100	1		1	3	0	1	12	0	16	MCR, MCT, WFS x2, PSL(PMC, FSS, ISS)	
k1mc	C Control	1		FMC-Area	9	100	1		1	2	1	0	6	2	11	MCI, MCO, MCE	
k1mmt	C Control	1		FMC-Area	9	100	1		0	1	1	0	11	1	14	MMT1, MMT2	
k1pr	C Control	1		P-Area	7	100	2		1	2	4	0	8	3	17	PRM, PR3	
k1pr2	C Control	1		B-Area	4	75	1		1	2	2	0	4	2	10	PR2	
k1bs	C Control	1		B-Area	4	75	1		1	2	2	0	5	2	11	BS	
k1sr2	C Control	1		B-Area	4	75	1		1	2	2	0	5	2	11	SR2	
k1sr3	C Control	1		S-Area	5	50	1		1	2	2	0	5	2	11	SR3	
k1srm	C Control	1		S-Area	5	50	1		1	2	2	0	5	2	11	SRM	
k1ommt	C Control	1		S-Area	5	50	2		0	2	2	0	8	2	14	OMMT1, OMMT2, STM1, STM2	
k1omc	C Control	1		S-Area	5	50	1		1	2	1	1	4	1	9	OMC+OFI	
k1ix1	C Control	1		XFrontVI (XFrontCryoBack)	40(22)	120	2		1	2	2	0	5	2	11	ITMX	for Type A & C
k1iy1	C Control	1		YFrontVI (YFrontCryoBack)	44(32)	120	2		1	2	2	0	5	2	11	ITMY	for Type A & C
k1ex1	XEndVIPre (XEndMec)	61(54)		XEndVI (XEndCryoARsideDuct)	60(51)	50	1	1	0	3	2	0	5	2	12	ETMX	for Type A & C
k1ex2	XEndVIPre (XEndMec)	61(54)		XEndVI (XEndCryoARsideDuct)	60(51)	50	1	1	0	1	1	0	8	1	11	BRT, TRX	
k1ey1	YEndVIPre (YEndMec)	81(74)		YEndVI (YEndCryoARsideDuct)	80(71)	50	1	1	0	3	2	0	5	2	12	ETMY	for Type A & C
k1ey2	YEndVIPre (YEndMec)	81(74)		YEndVI (YEndCryoARsideDuct)	80(71)	50	1	1	0	1	1	0	8	1	11	BRT, TRY	
k1lsc	C Control	1		?	?	75	1	1	1	3	0	0	13	0	16	ASRF, REFL, POX, POY, POP, POS	
k1asc1	C Control	1		?	?	75	1	1	1	3	0	0	14	0	17	WFSAS, WFSREFL, WFSPOX	
k1asc2	C Control	1		?	?	75	1	1	1	2	0	0	8	0	10	WFSAS, WFSREFL, WFSPOX	
k1aux	C Control	1		?	?	100	1		1	2	0	?	0	0	2	GRX, GRY	
k1pcx	X arm center	N/A		X arm center	?	2	3		0	1	0	0	0	0	1	PEM	
k1pcy	Y arm center	N/A		Y arm center	?	2	3		0	1	0	0	0	0	1	PEM	
					Total		31	7	15	46	29	2	144	29	250		
					Max				18	60	40		99		17/ea.		

JGW-G1201105

- 19 RT Front-End will be used in iKAGRA, and 27 in bKAGRA.
- 46 of 60 ADC and 29 of 40 DAC are assigned.
- Needs 173 Binary Out module. Only 99 we have now. Using Acromag 96ch slow BO?

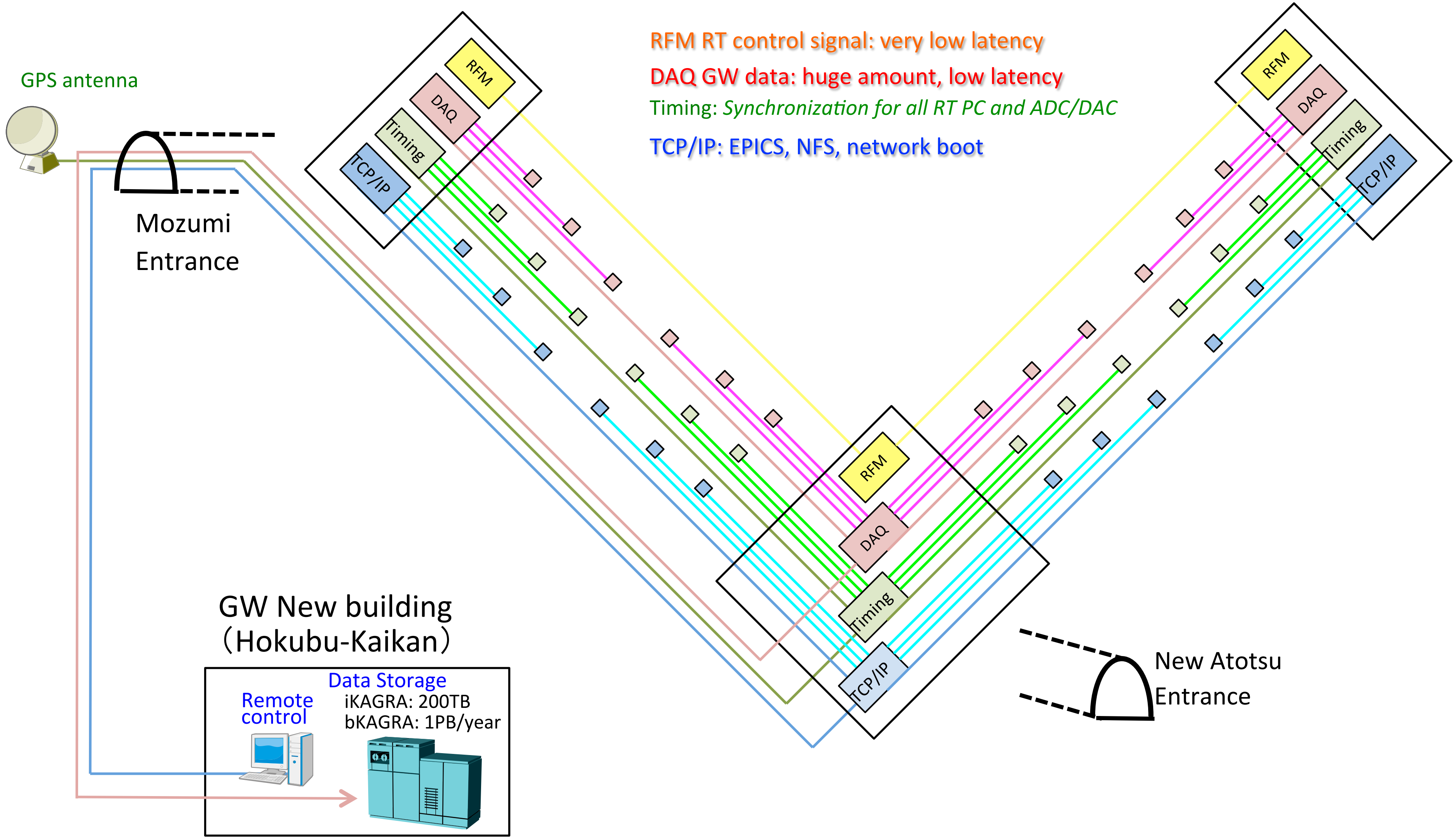
Connection to Field racks



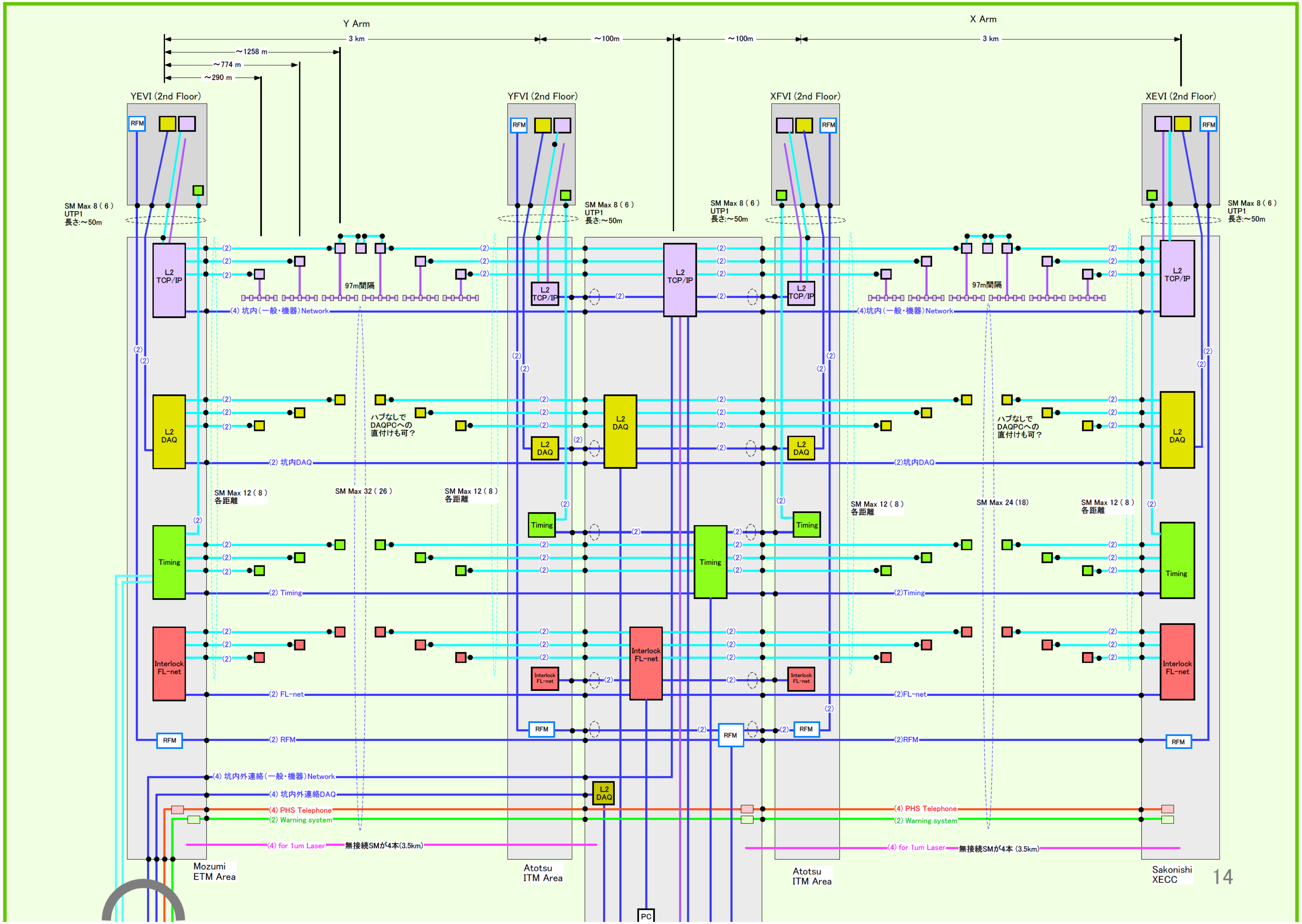
- Computer rack
- DC power supply rack
- Field rack(IO chassis, ADC, DAC, AA/AI, circuits)
- Mini field rack (PC, IO chassis, AA/AI, circuits, DC power supply)
- End rack (PC, DC power)

Remove noisy AC100V from experimental room

Network design



SM Fiber (1G or 10G) Net
● スプライスボックス接続(予定)
SM Fiber (1G) Net
SM Fiber Warning System
1G Metal
SM Fiber PHS System
SM Fiber for 1um Laser
HUB, Timing, DAQ, FL-net Instrument



Channels list

- Assigned PSL, IOO, MIF, VIS (except for OMC, OMMT, BRT)
- Next task: estimation for number/length of cables (D-SUB, RF, fiber)

[JGW-T1201105]

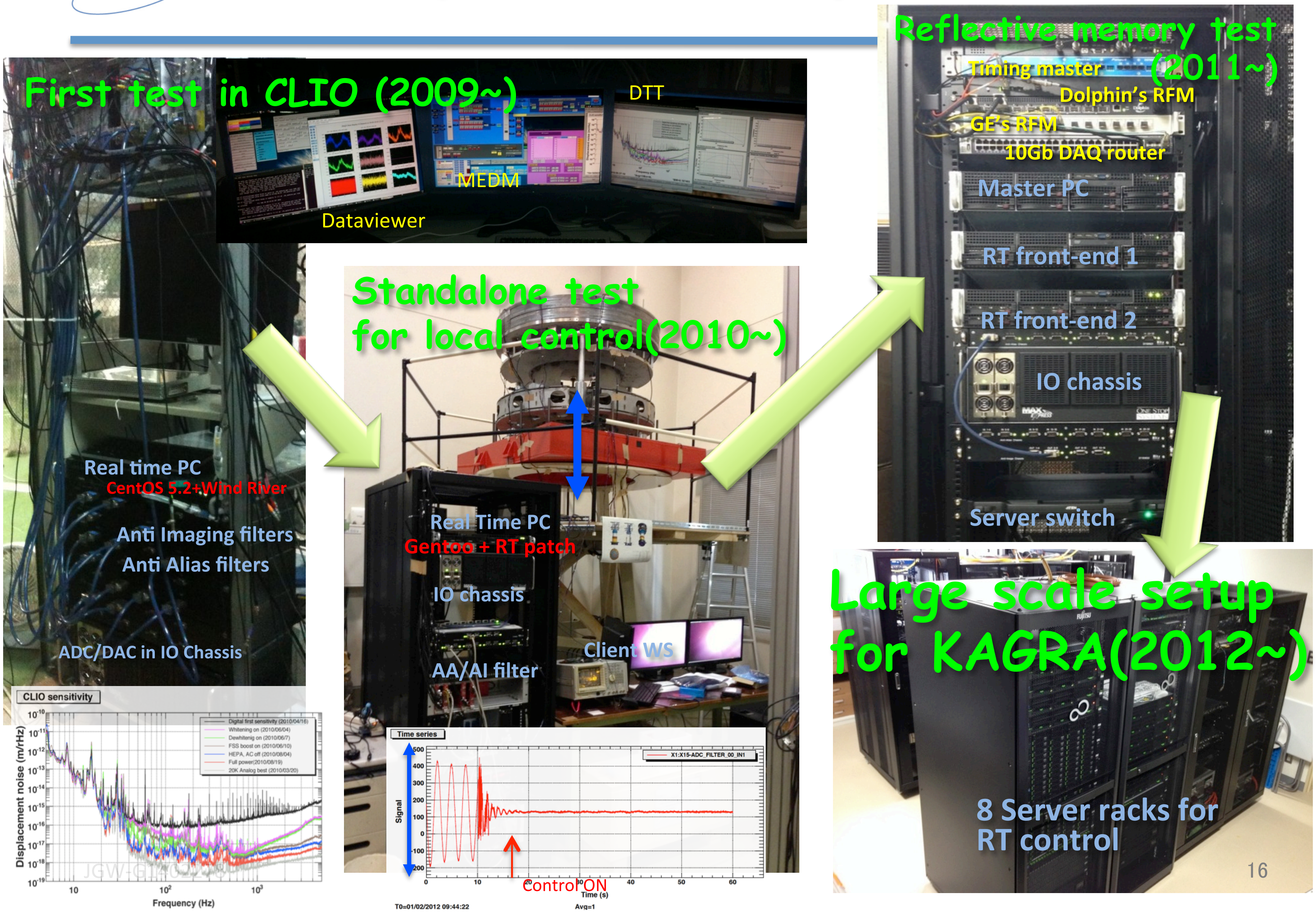
Signal channel list 2014/3/18

JGW-T1201105
Osamu Miyakawa

Reference: JGW-T1100689

Subsystem	Location	Instrument	Signal description	Ch. Name	Card No.	Ch	Whitening	ISC whitening	Dewhitening	RT model	RT PC name
PSL	FSS	RF PD	I-phase	K1:PSL-FSS_REFL_I	ADC1	1		1		k1psl	k1io
PSL	FSS	RF PD	Q-phase	K1:PSL-FSS_REFL_Q	ADC1	2		1		k1psl	k1io
PSL	PMC	RF PD	I-phase	K1:PSL-PMC_REFL_I	ADC1	3		1		k1psl	k1io
PSL	PMC	RF PD	Q-phase	K1:PSL-PMC_REFL_Q	ADC1	4		1		k1psl	k1io
PSL	FSS	DC PD	DC	K1:PSL-FSS_REFL_DC	ADC1	5		1		k1psl	k1io
PSL	FSS	DC PD	DC	K1:PSL-FSS_TR_DC	ADC1	6		1		k1psl	k1io
PSL	PMC	DC PD	DC	K1:PSL-PMC_REFL_DC	ADC1	7		1		k1psl	k1io
PSL	PMC	DC PD	DC	K1:PSL-PMC_TR_DC	ADC1	8		1		k1psl	k1io
PSL	ISS	DC PD	DC	K1:PSL-ISS_DC	ADC1	9		1		k1psl	k1io
PSL			spare		ADC1	10		1		k1psl	k1io
PSL			spare		ADC1	11		1		k1psl	k1io
PSL			spare		ADC1	12		1		k1psl	k1io
PSL			spare		ADC1	13				k1psl	k1io
PSL			spare		ADC1	14				k1psl	k1io
PSL			spare		ADC1	15				k1psl	k1io
PSL			spare		ADC1	16				k1psl	k1io
PSL	BENCH	DC QPD	injection beam pointing monitor, quadrature 1	K1:PSL-BENCH_OUT_QPD1_Q1	ADC1	17		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam pointing monitor, quadrature 2	K1:PSL-BENCH_OUT_QPD1_Q2	ADC1	18		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam pointing monitor, quadrature 3	K1:PSL-BENCH_OUT_QPD1_Q3	ADC1	19		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam pointing monitor, quadrature 4	K1:PSL-BENCH_OUT_QPD1_Q4	ADC1	20		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam position monitor, quadrature 1	K1:PSL-BENCH_OUT_QPD2_Q1	ADC1	21		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam position monitor, quadrature 2	K1:PSL-BENCH_OUT_QPD2_Q2	ADC1	22		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam position monitor, quadrature 3	K1:PSL-BENCH_OUT_QPD2_Q3	ADC1	23		1		k1psl	k1io
PSL	BENCH	DC QPD	injection beam position monitor, quadrature 4	K1:PSL-BENCH_OUT_QPD2_Q4	ADC1	24		1		k1psl	k1io
PSL			spare		ADC1	25				k1psl	k1io
PSL			spare		ADC1	26				k1psl	k1io
PSL			spare		ADC1	27				k1psl	k1io
PSL			spare		ADC1	28				k1psl	k1io
PSL			spare		ADC1	29				k1psl	k1io
PSL			spare		ADC1	30				k1psl	k1io
PSL			spare		ADC1	31				k1psl	k1io
PSL			reserved for 1PPS		ADC1	32				k1psl	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 1 I-phase	K1:IOO-MCR_QPD_G1_Q1_I	ADC2	1		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 1 Q-phase	K1:IOO-MCR_QPD_G1_Q1_Q	ADC2	2		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 2 I-phase	K1:IOO-MCR_QPD_G1_Q2_I	ADC2	3		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 2 Q-phase	K1:IOO-MCR_QPD_G1_Q2_Q	ADC2	4		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 3 I-phase	K1:IOO-MCR_QPD_G1_Q3_I	ADC2	5		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 3 Q-phase	K1:IOO-MCR_QPD_G1_Q3_Q	ADC2	6		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 4 I-phase	K1:IOO-MCR_QPD_G1_Q4_I	ADC2	7		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 1 Quadrature 4 Q-phase	K1:IOO-MCR_QPD_G1_Q4_Q	ADC2	8		1		k1io	k1io
IOO	MCR	DC QPD	Gouy phase 1 Quadrature 1 DC	K1:IOO-MCR_QPD_G1_Q1_DC	ADC2	9				k1io	k1io
IOO	MCR	DC QPD	Gouy phase 1 Quadrature 2 DC	K1:IOO-MCR_QPD_G1_Q2_DC	ADC2	10				k1io	k1io
IOO	MCR	DC QPD	Gouy phase 1 Quadrature 3 DC	K1:IOO-MCR_QPD_G1_Q3_DC	ADC2	11				k1io	k1io
IOO	MCR	DC QPD	Gouy phase 1 Quadrature 4 DC	K1:IOO-MCR_QPD_G1_Q4_DC	ADC2	12				k1io	k1io
IOO			spare		ADC2	13				k1io	k1io
IOO			spare		ADC2	14				k1io	k1io
IOO			spare		ADC2	15				k1io	k1io
IOO			spare		ADC2	16				k1io	k1io
IOO	MCR	RF QPD	Gouy phase 2 Quadrature 1 I-phase	K1:IOO-MCR_QPD_G2_Q1_I	ADC2	17		1		k1io	k1io
IOO	MCR	RF QPD	Gouy phase 2 Quadrature 1 Q-phase	K1:IOO-MCR_QPD_G2_Q1_Q	ADC2	18		1		k1io	k1io

Development of control system for KAGRA

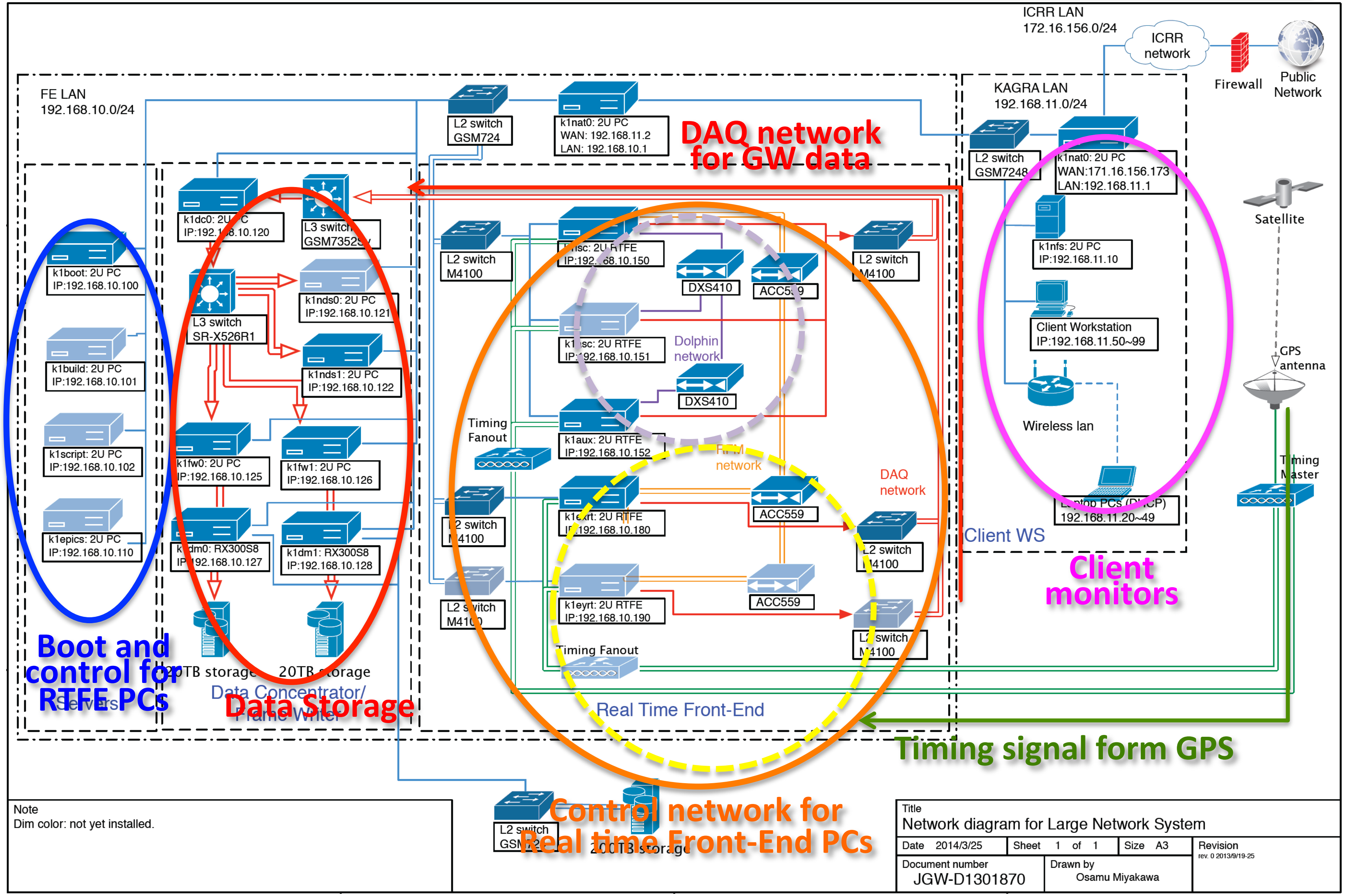


Objectives for Large Network System(LNS)

1. Very close system as real KAGRA control system, and easy installation into mine.
2. Operation test with multiple computers.
   - Real Time Front-End computers
   - Servers (boot, model building, scripting, NFS)
3. Data acquisition test.
   - Huge amount of data, latency
4. Stable operation.
   - Long term operation test
   - Preparations for power shutdown and power recovery
5. Redundancy.
   - Dual path for DAQ network
   - Dual power supply for servers being equipped with hard drives

- What we cannot test at LNS.
  - Network connection through 3km arms
  - Full scale Real Time network with ~30 RT computers

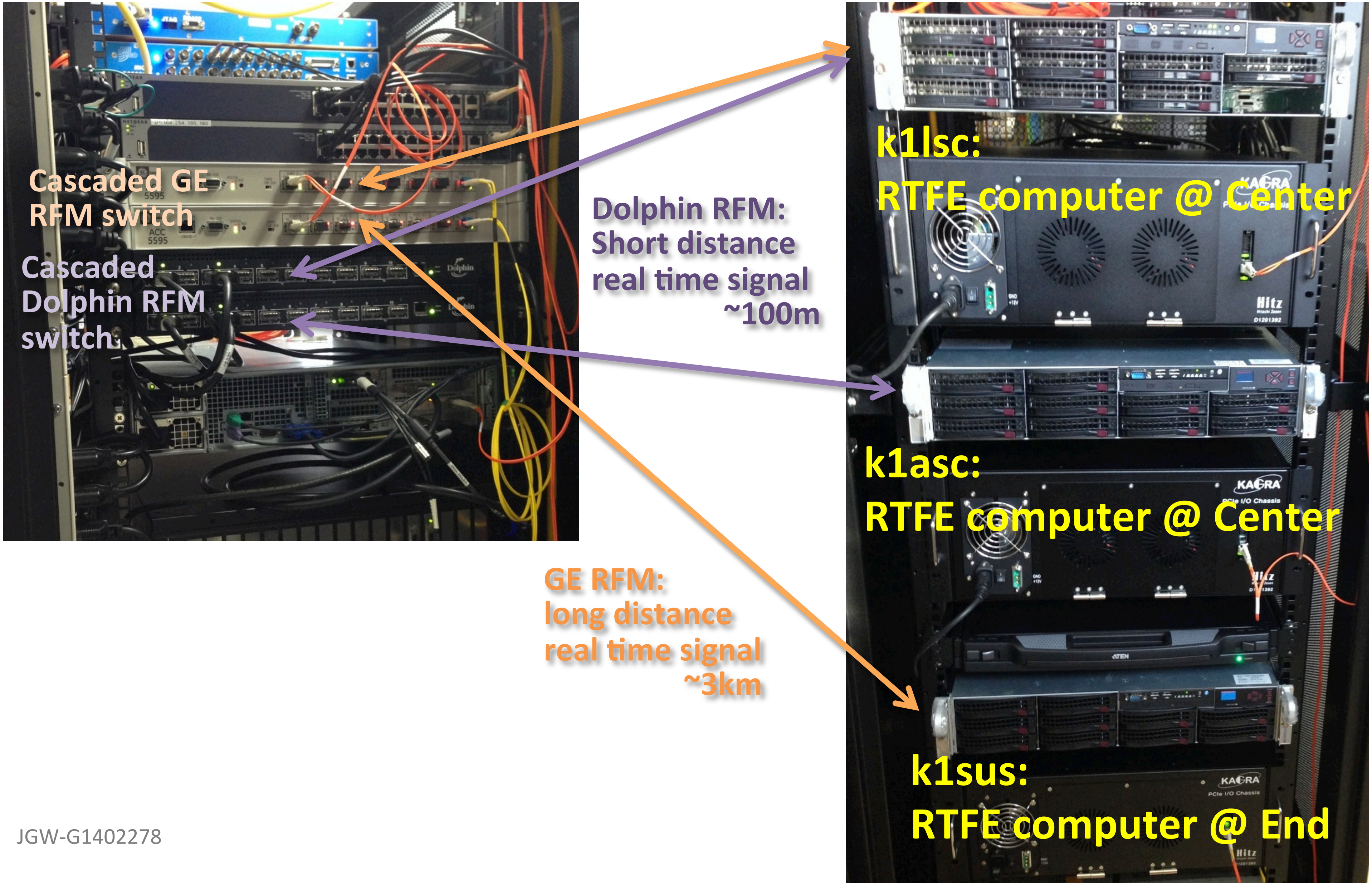
Diagram of Large Network System



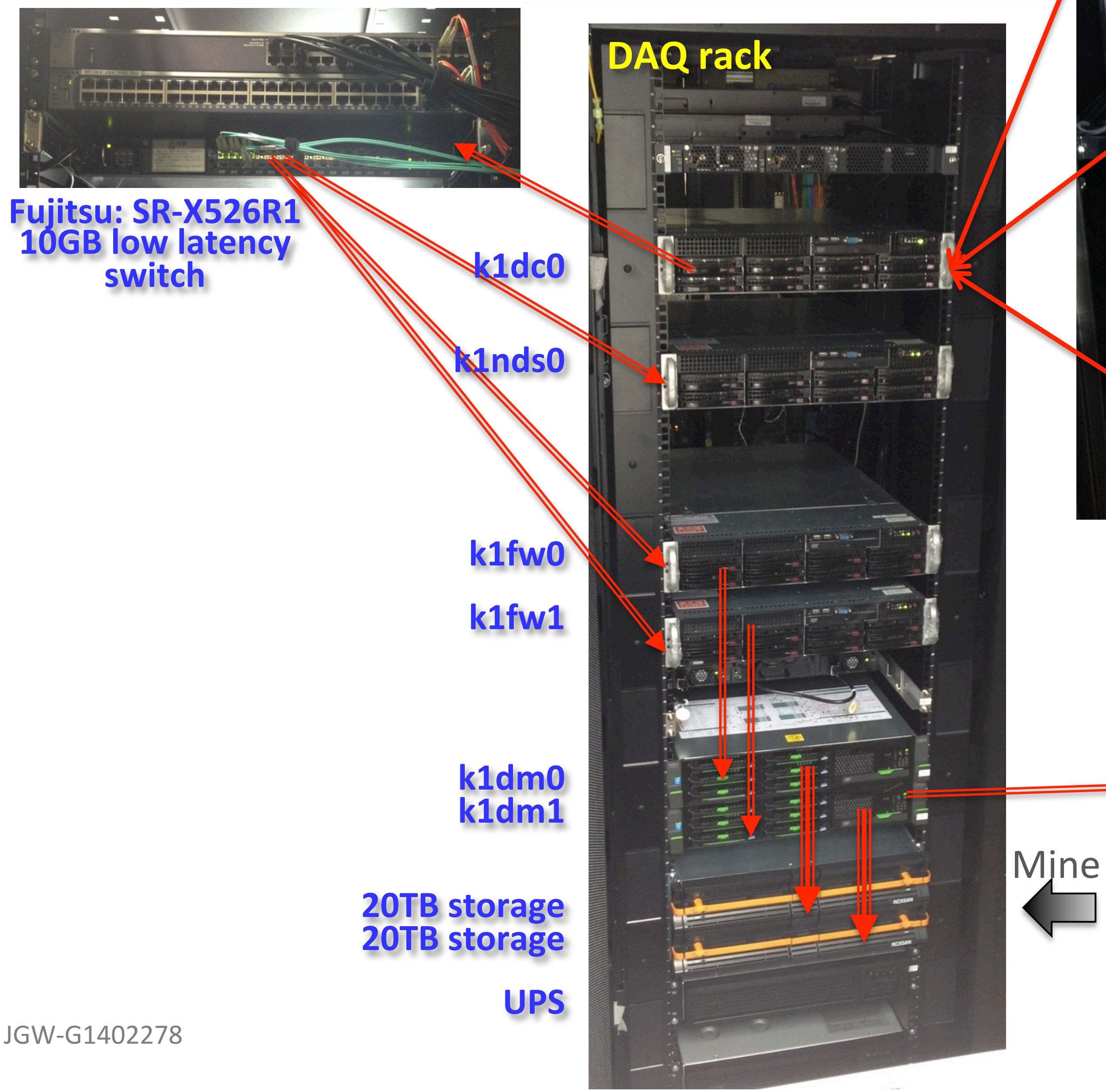
Note
Dim color: not yet installed.

Title			
Network diagram for Large Network System			
Date 2014/3/25	Sheet 1 of 1	Size A3	Revision rev. 0 2013/9/19-25
Document number JGW-D1301870	Drawn by Osamu Miyakawa		

Control signal network for Real Time Front-end using ReFlective Memory technology

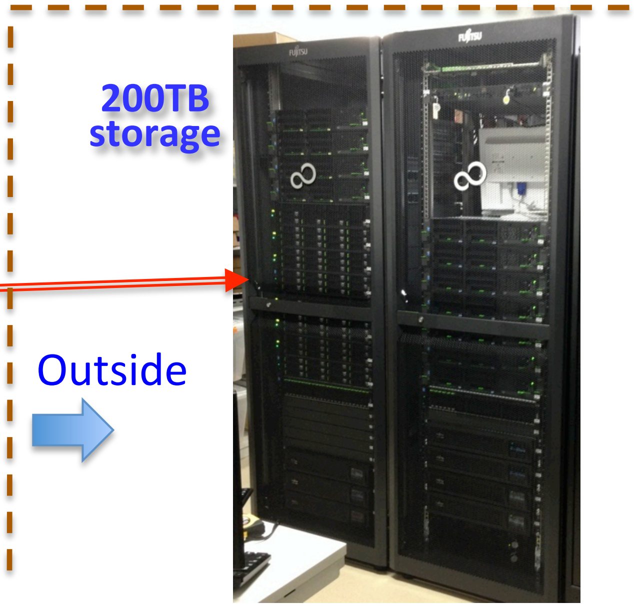


DAQ network



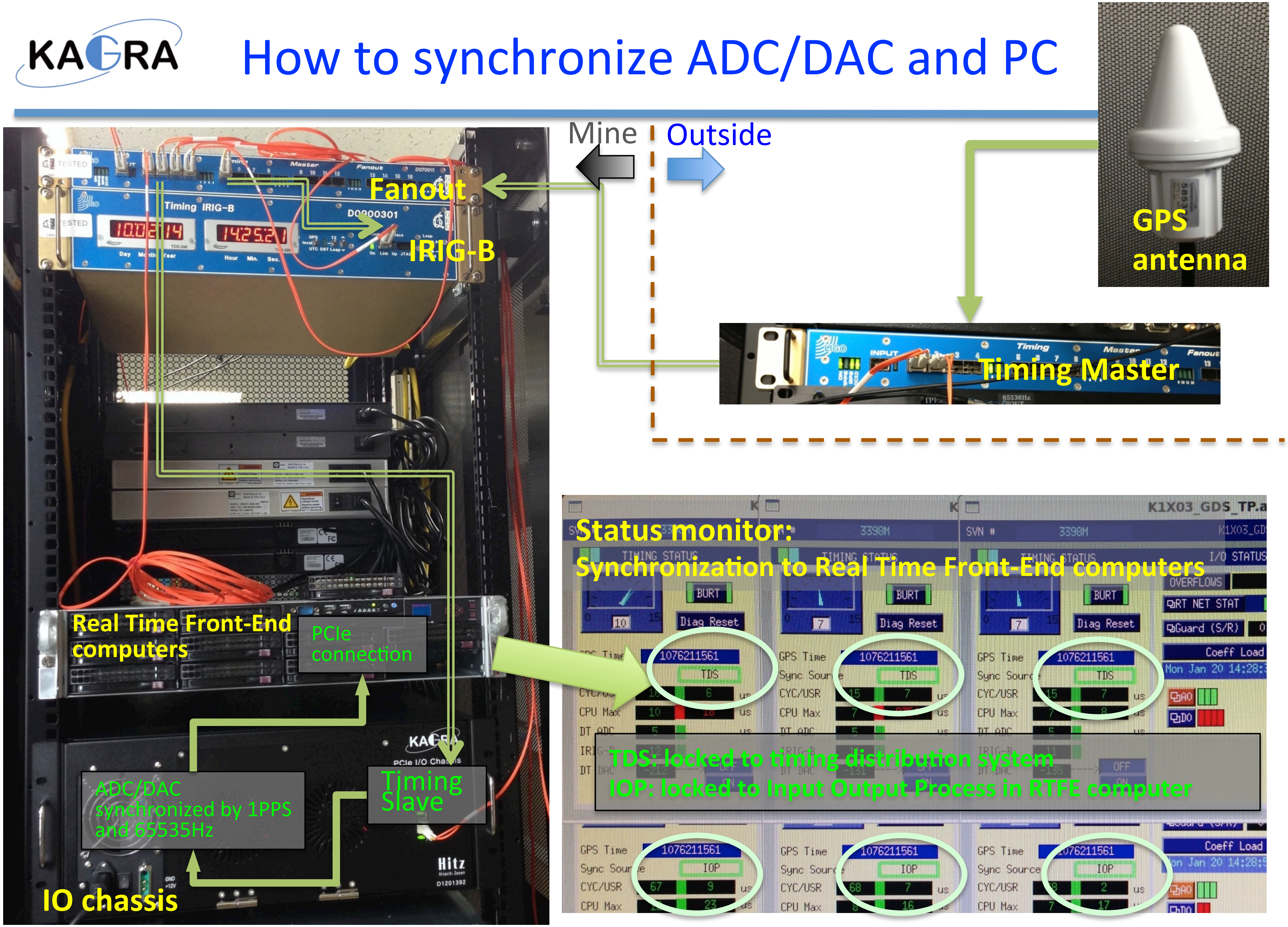
Fujitsu: SR-X526R1
10GB low latency
switch
DAQ rack
k1dc0
k1nds0
k1fw0
k1fw1
k1dm0
k1dm1
20TB storage
20TB storage
UPS
Mine

Real Time Front-End
computers

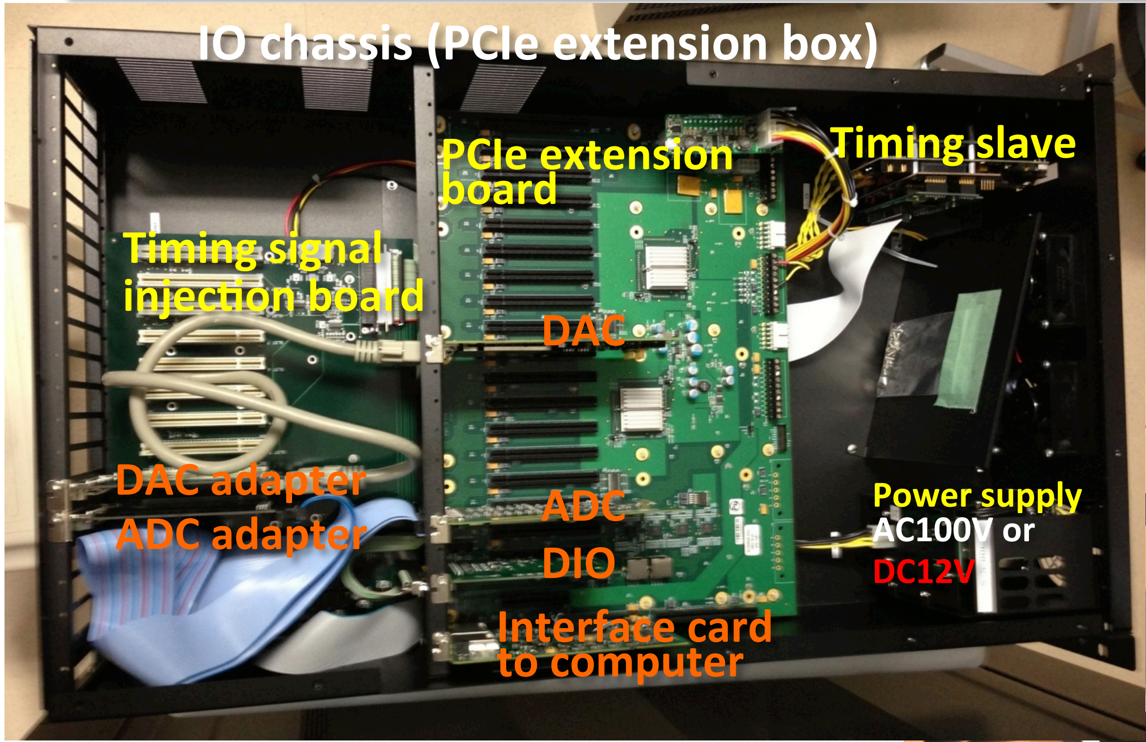


Outside
200TB
storage

How to synchronize ADC/DAC and PC

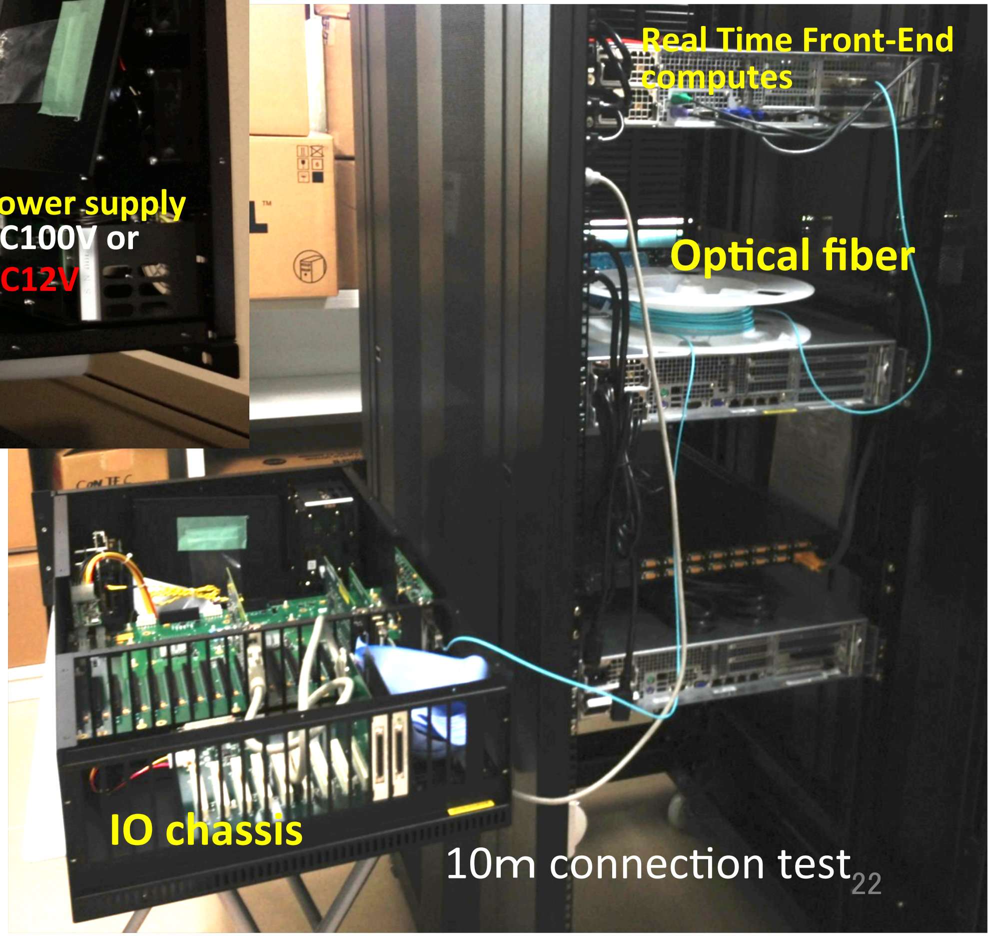


Connection between RTFE computer and PCIe extension chassis



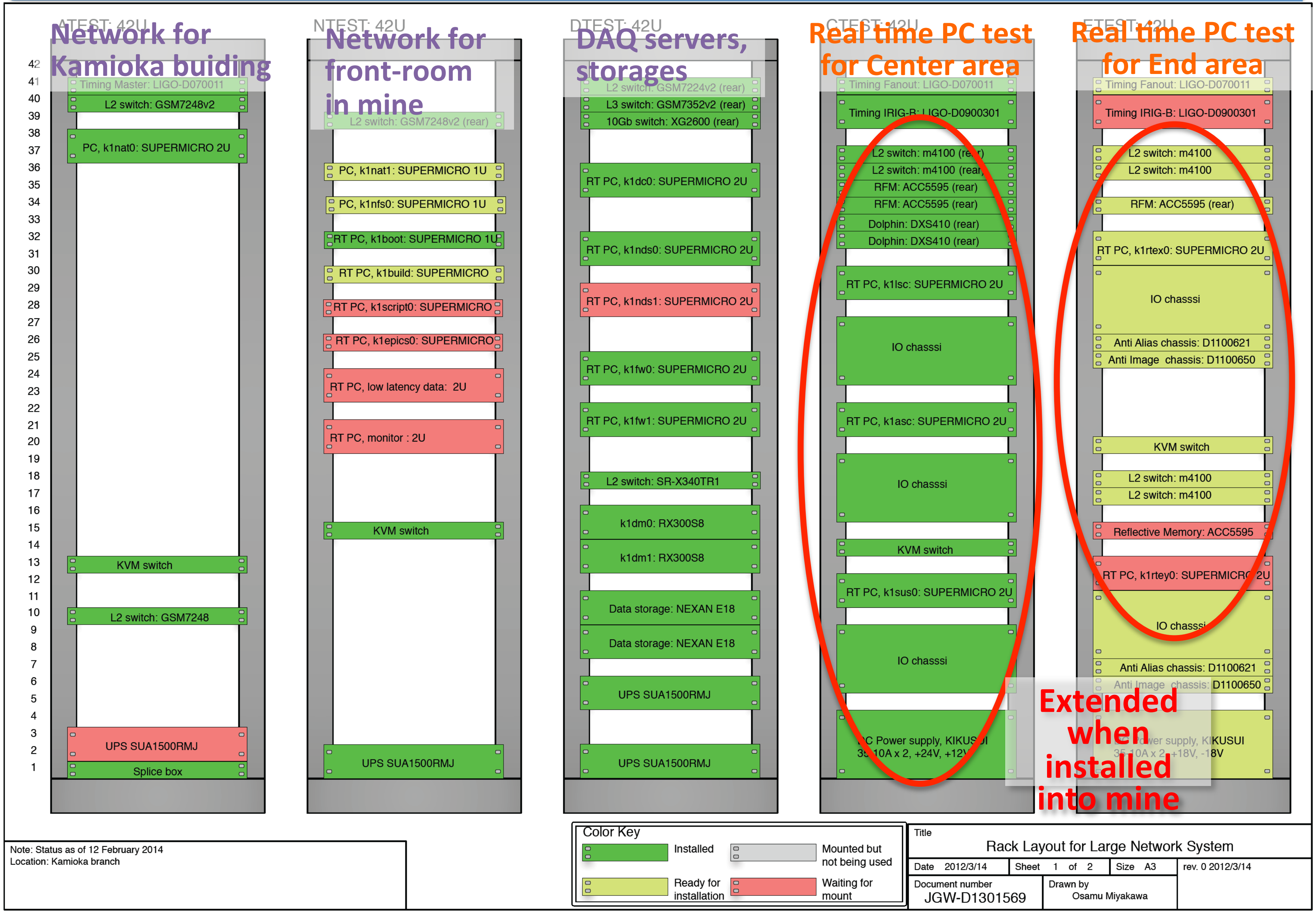
Total 31 chassis manufactured

for bKAGRA

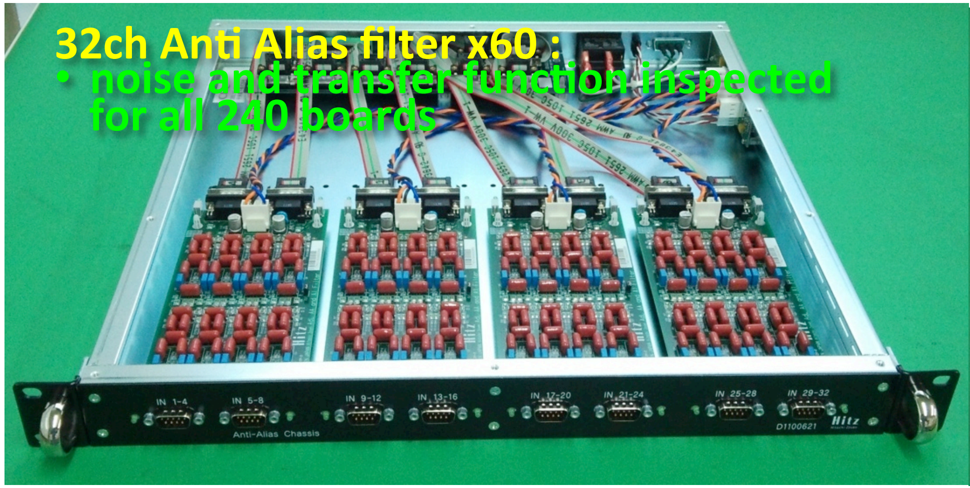


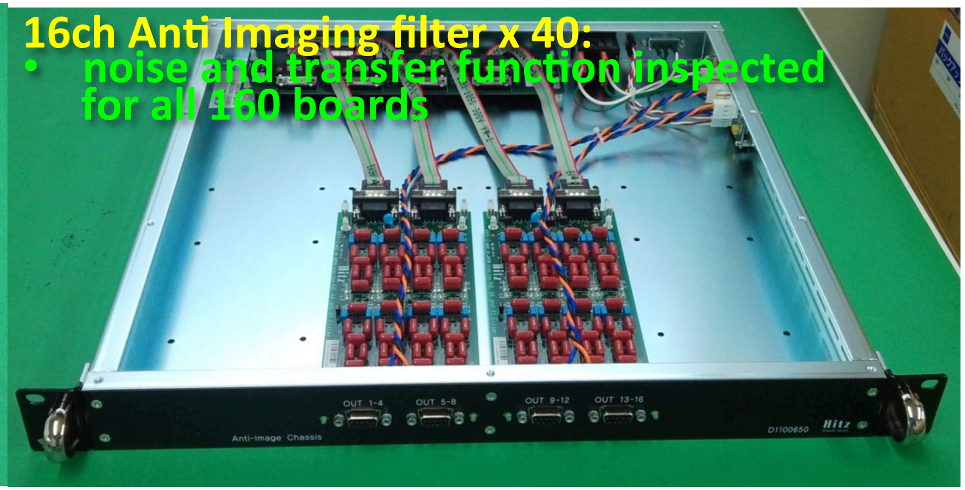
- Remote connection up to 100m using optical fiber will be tested soon.

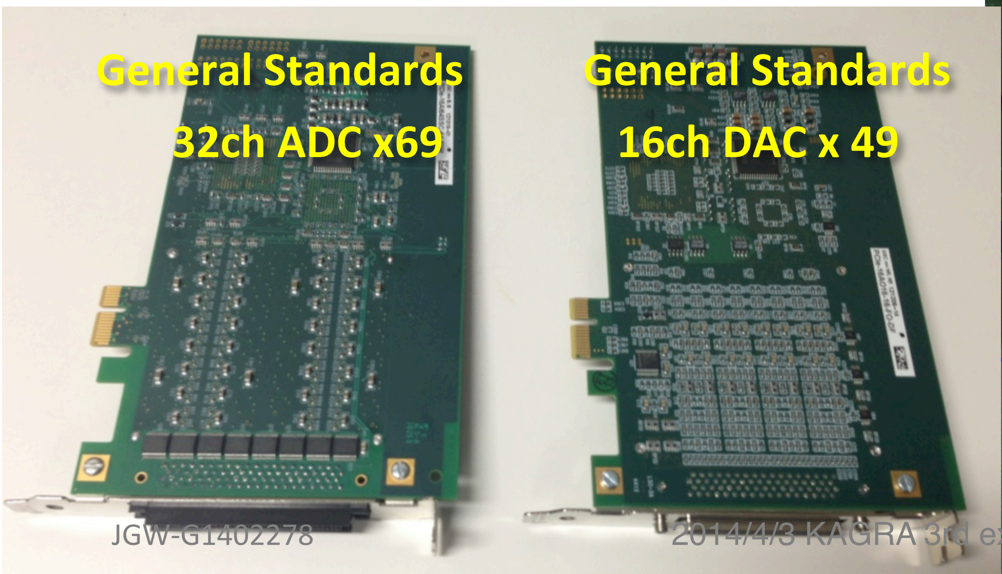
Rack layout for Large Network System



DAQ items







All AA/AI manufactured for bKAGRA

KAGRA

Instrument Control

Objective

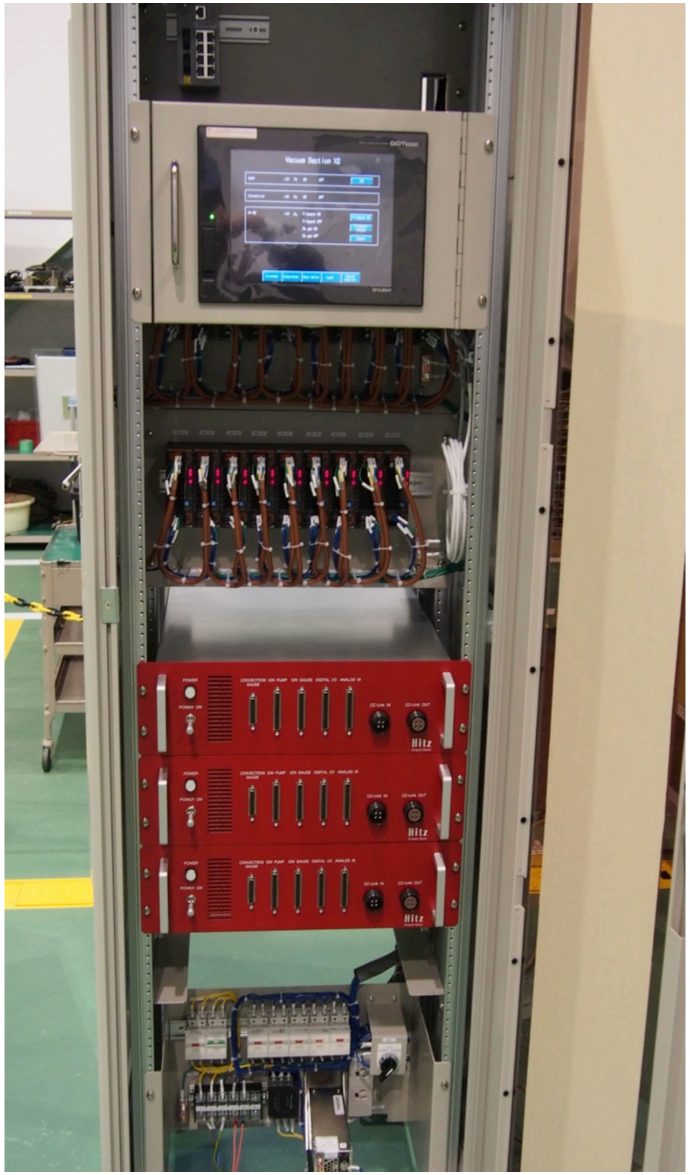
- Monitor the status of various instruments throughout the KAGRA site including environmental monitors.
- Remotely manipulate some instruments.
- Automatically shut the gate valves and the laser in case of an accident.

Implementation

- Industrial PLC for robust operation
- Three core modules (center, X-end, Y-end)
- 30 I/O modules along each arm
- EPICS translator to interface for user interface

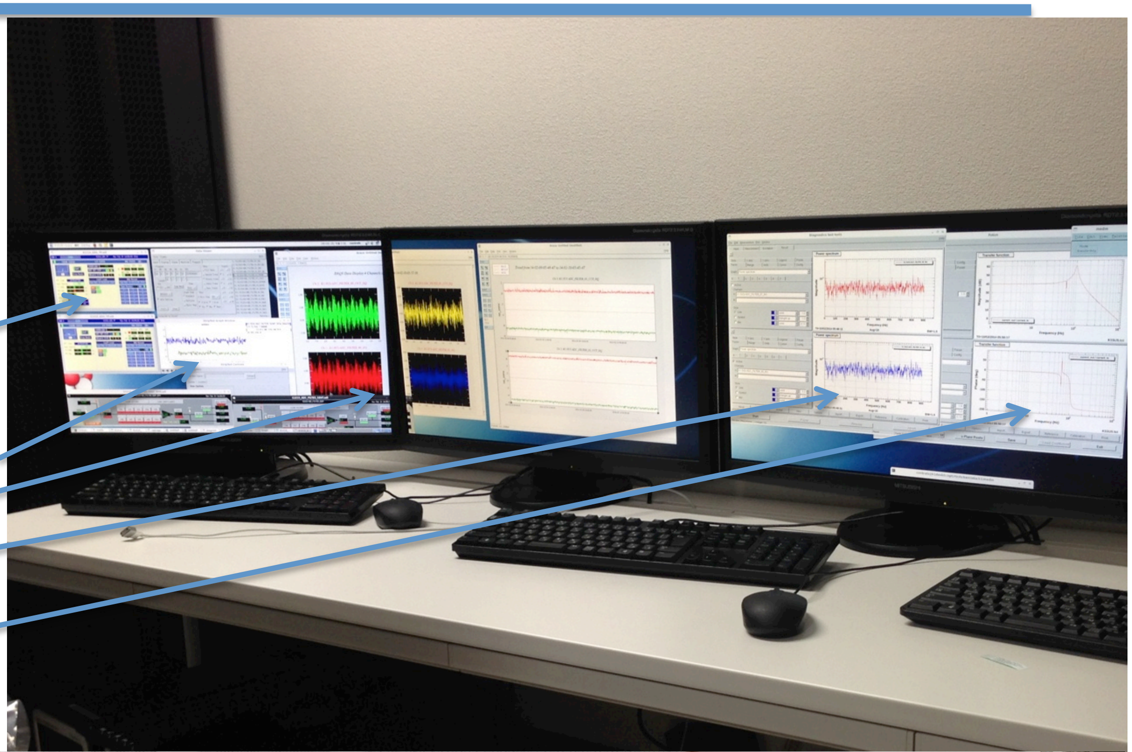
Status

- Central area core module: Delivered
- X-end, Y-end core modules: Delivered
- 6 I/O modules: Delivered
- 54 I/O modules: To be purchased



Client workstation in control room

- 3 heads client workstations in the control room
- Direct access to 2weeks past frame data in 20TB storage.
- Control software:
  - MEDM (EPICS GUI)
  - StripTool (long term EPICS ch viewer)
  - Dataviewer (oscilloscope)
  - DTT (spectrum analyzer)
  - Foton (digital filter composer)
  - TDS commands (script)



KAGRA Storage in the current/new building at Kamioka

AA: 1U x 66
AI: 1U x 46
IO chassis: 4U x 31
RT PC: 2U x 28
Server PC: 1U x 11
DC power supply: 4U x 75

Total ~600U = 42U x 15 racks

Total number of racks in the mine will be ~30.

Analog electronics chassis will be continuously made and stored in the racks until installation.

Remaining issues

- Connection between RTFE and IO chassis through 100m fiber since Trenton backplane does not support GEN2 connection.
  - One Stop System answered they will patch GEN1 mode to their GEN2 interface cards.
- Inspection of ADC/DAC
  - Some excess noise channels seen on ADC
- Timing injection to data concentrator (k1dc0)
  - Synchronization error on DTT
- Fixing mapper on Myrinet
  - No DAQ stream
- Slow start of Myrinet cards on frame writers causes no connection to frame data when booted.
- Build, script, epics, NFS and NAT servers

Summary

- Almost of core technologies for real time control have been implemented with LIGO CDS support.
- Some remaining items and some miner issues to be fixed.