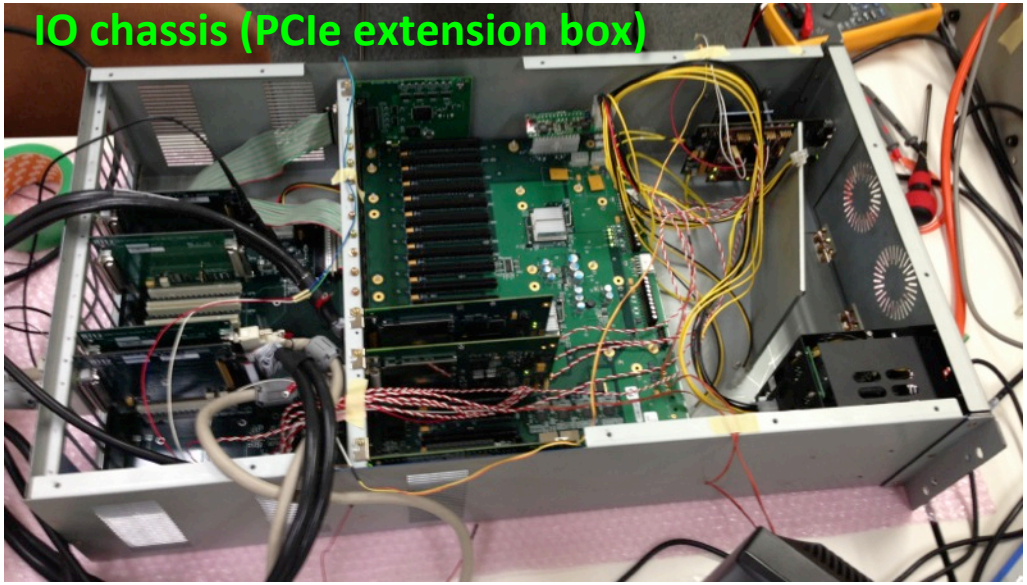
Main activity of DGS and AEL

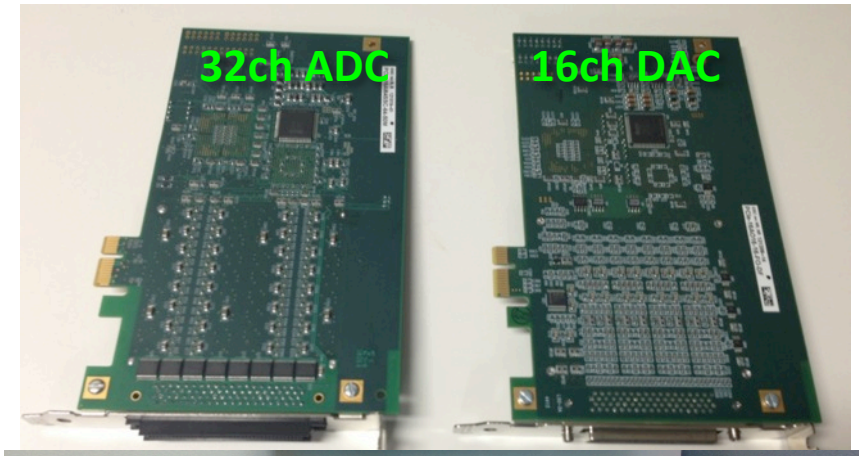
1. Whole DAQ system (ADC, DAC, AA, AI, IO chassis, not including computers, networks) for bKAGRA was ordered and partially inspected.
2. Updating RTS (Real Time Software) from 2.1.4 to 2.5.2 (the latest is 2.6.2).
   - Updated STDA ,SNS at Kamioka, VIS at Kashiwa. Planned update at NAO and Hongo.
3. K1 (instead of X1) as channel name is available now.
4. Some measurements, multi channel ADC noise, DAC noise, delay by RFM, will be useful for inspection later.
5. Construction for LNS (large network system) at Kamioka
6. S-number (serial number) system started at JGWDoc to manage circuit boards, chassis, PCs etc.

DAQ items

- IO chassis x 25: manufactured
- ADC x 60 (x32ch): ordered
- DAC x 40 (x16ch): ordered
- Anti alias x60: manufactured
- Anti image x40: manufactured
- Whitening filter x75: being designed

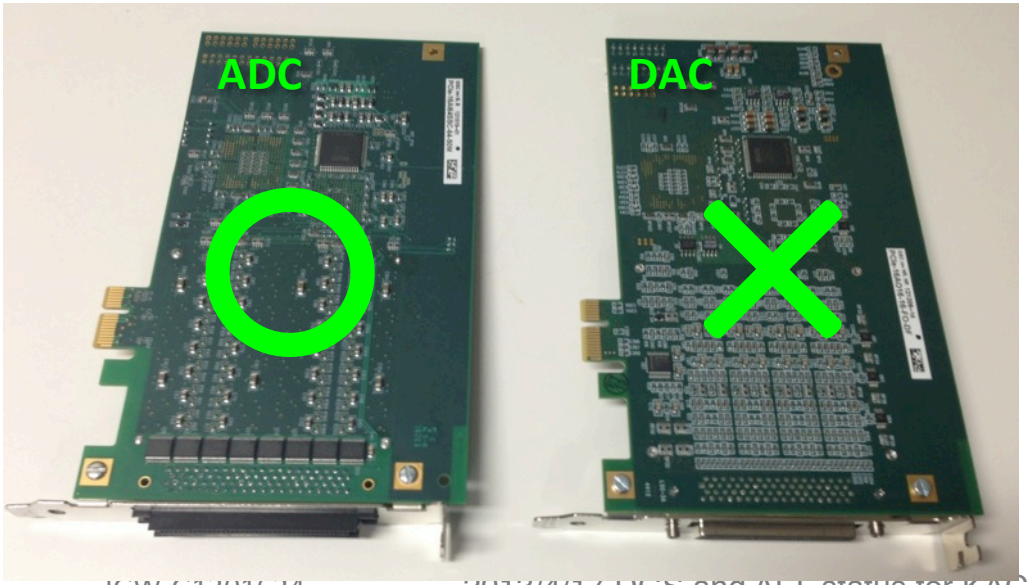
Preparing for bKAGRA observation





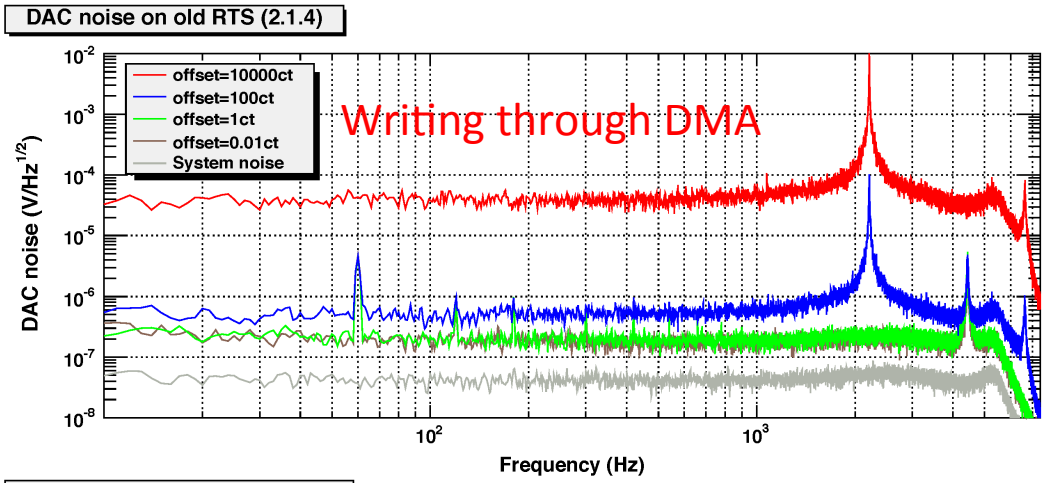
Troubles on DAC

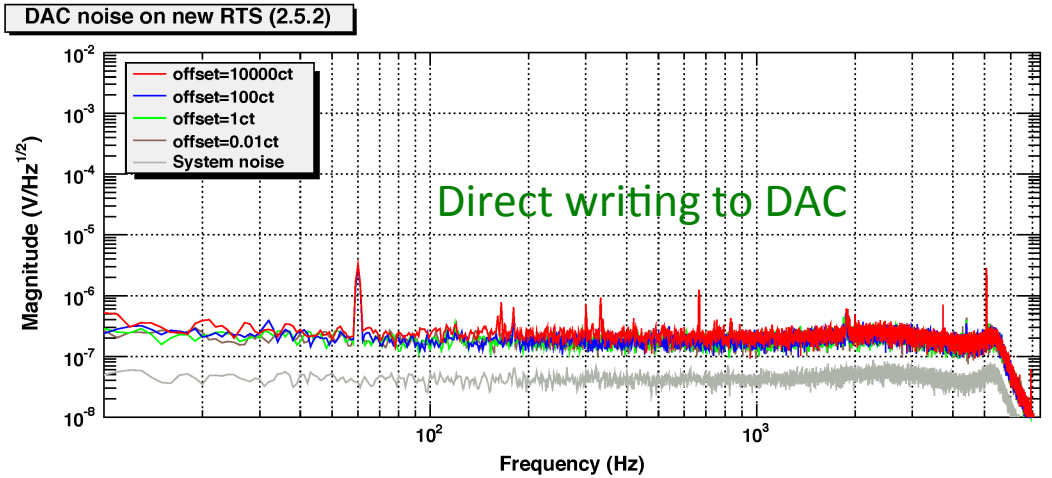
- 2kHz, 5kHz peeks were seen from DAC on VIS, but verified no such peeks in Kamioka system -> some connection problem?
- DAC noise floor increased by DC offset on DAC
- New PCIe based DAC being ordered did not work with current RTS version 2.1.4
  - No output voltage
  - Recognized in hardware, or software
  - Old DAC works well
  - Old/new ADC works well



DAC output

- Problem at the very last stage to wirte to DAC through DMA(Direct Memory Access)
- Fixed by wirting to DAM
- New DAC works with the direct writing.





Controller.c:

```
#ifdef DIRECT_DAC_WRITE
            dac16bitPtr->ODB = dac_out;;
#else
          // DMA Write data to DAC module
            if(dacWriteEnable > 4) gsaDacDma2(jj,cdsPciModules.dacType[jj],dacBufOffset);
#endif
```

←Direct writing to DAC

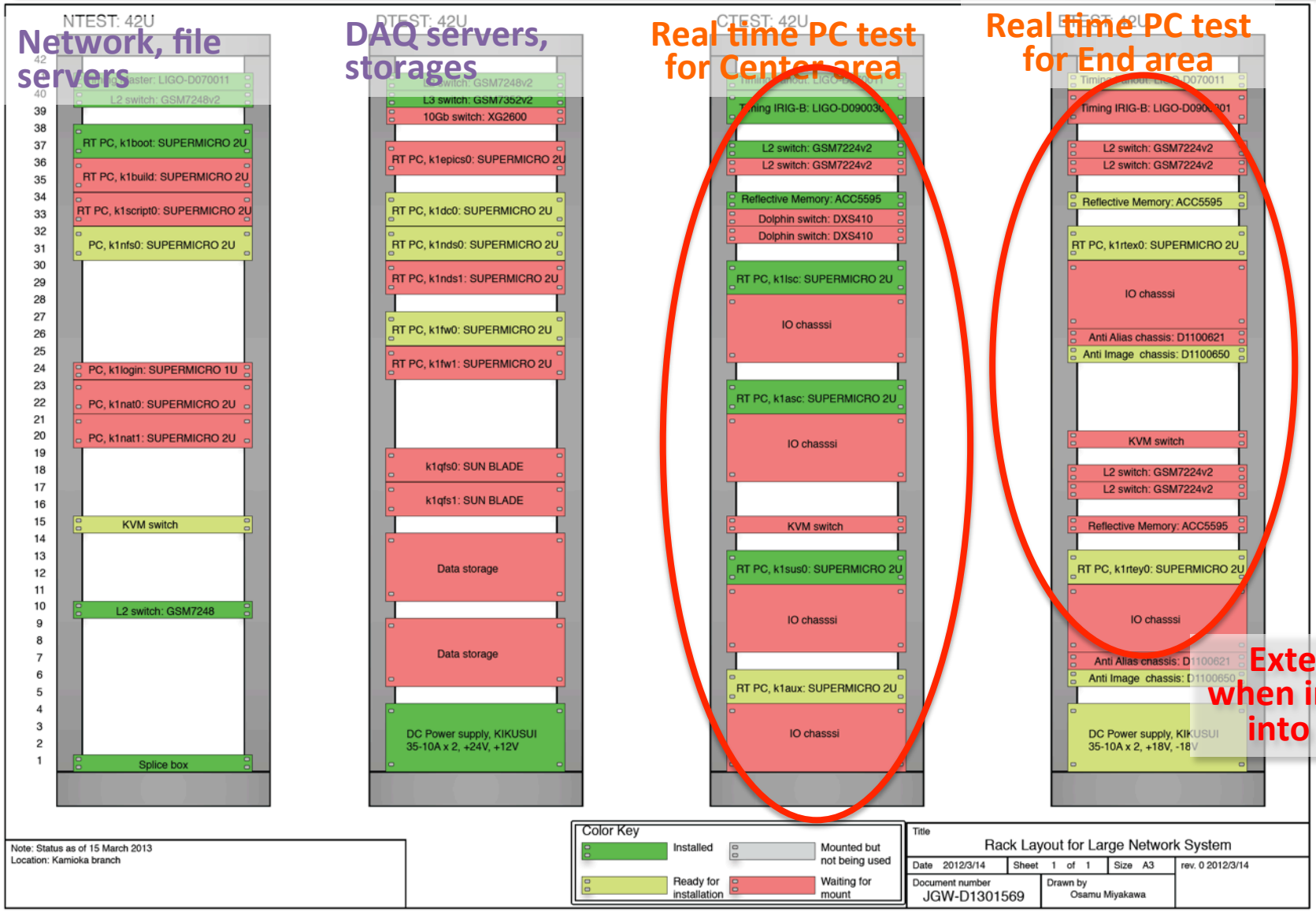
↓DMA causes troubles

Items for Real Time control

	Stand alone system FY2010-	Small network test FY2011	Large network test FY2012, 2013	Full system FY2014~
Real time PC	1	2	~6	~25
IO chassis	1	0	~6	~25
Servers	0	1	15	15
ADC	1	2	~10	~70
DAC	1	0	~10	~35
Binary Output	1	0	~10	~100
Long Reflective memory switch	0	1	3	3
Short Reflective memory switch	0	1	2	2
DAQ switch	0	1	2	2
Timing switch	0	1	4	4
IRIG-B switch	0	0	1	3
Data storage	1TB	2TB	~20TB	~500TB

Red: new items
Green: increments

Rack layout for Large Network System



Number of necessary electronics

Orange: started discussion
Brown: testing
Blue: manufacturing
Green: done

Laser: 1 total: 1

Master laser controller

IOO: 15 variety, total :50 box

Rotator controller x2, Master oscillator x1, Frequency converter x5, Frequency doubler x1, RF distribution amplifier x10, Delay line phase shifter x5, EOM controller x5, PMC controller x1, FSS controller x1, VCO controller x1, ISS controller x1, IMC servo x1, OMC controller x1, PZT driver x10, Shutter x5

MIF: 9 variety, total 92 box

RF PD x20, DC PD x20, RF QPD x12, DC QPD x8, LSC I&Q demodulator x20, QPD 4ch I&Q demodulator x8, 2 x demodulator x1, CM servo x1, Green laser controller x2

VIS: 9 variety, total 508 box

LVDT driver x74, Coil driver for voice coil actuator x60, OSEM sensor/coil driver x110, Satelite amplifier x11, Stepper motor controller x44, Picomoror controller x44, Picomoror controller with load x11, GEO phone preamp x44, Dewhitening filter x110

Digital: 5 variety, total 230 box

IO chassis 25, Anti alias x60, Anti image x40, Binary output interface x30, Whitening filter x75

Current activities

- MIF: RF PD tested at Hongo

  whitening filter for 10 chassis (80ch) being ordered
- IOO: Frequency stabilized servo will be delivered on July, 2013
- VIS: 8ch LVDT driver will be implemented into 1U box on August, 2013