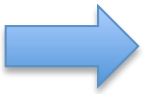
Schedule

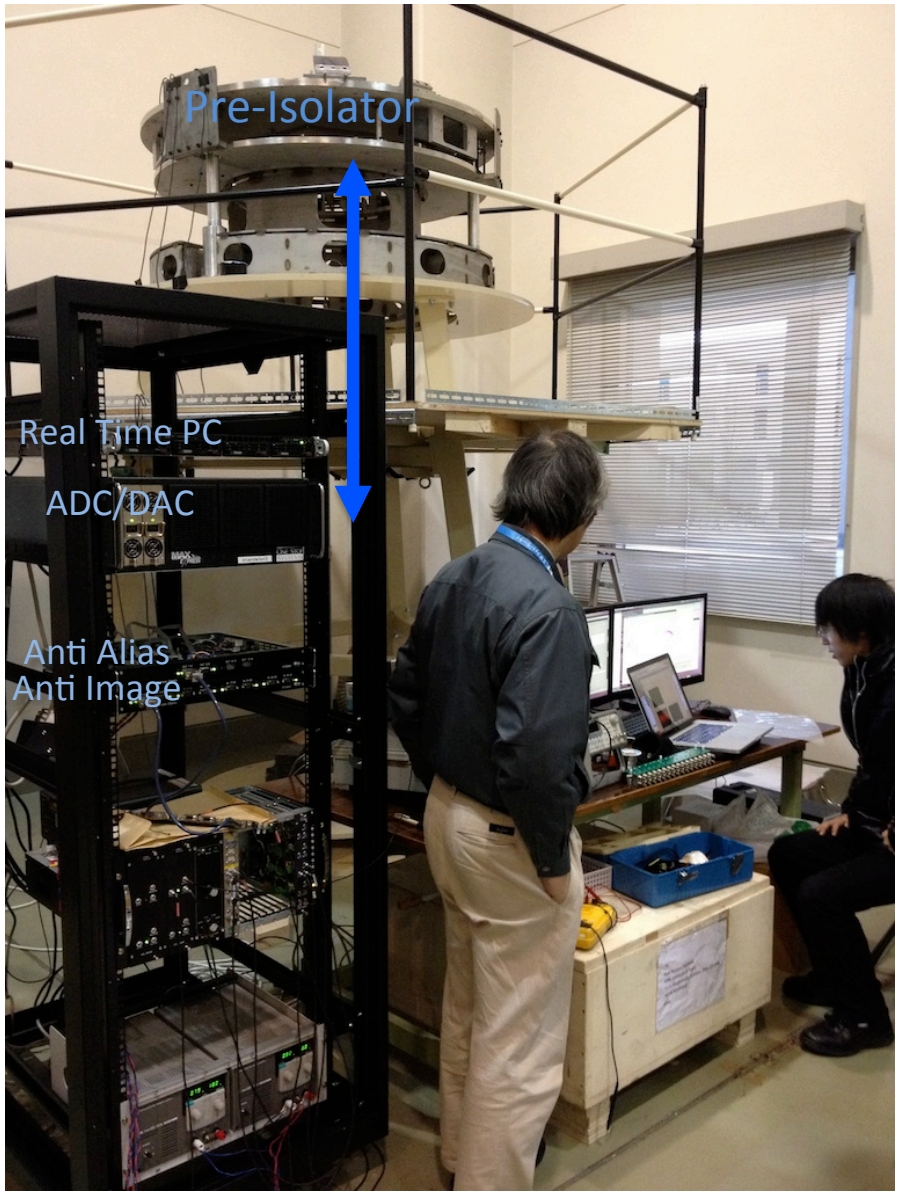
FY		2010				2011				2012				2013				2014				2015				2016			
Quarter		1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
Main Phase		Design								Tunnel								Vacuum				FPMI				RSE			
Prototype test	CLIO operation																												
	Data analysys test																												
Standalone system for subsystems	Hard/software setup																												
	Circuit																												
	Delivery																												
Article test	Small network																												
	Large network sytem																												
	Circuit																												
	Inspection																												
Full system	Installation																												
	Tuning																												
Upgrade	RSE																												
	Cryo																												

A. 2009-2010 prototype test @ CLIO (done)
   - Basic IFO operation and noise performance
B. 2011~ standalone system for subsystem (system: done, 2/5 delivered)
   - Data analysis, VIS, (IOO, CRY…)
C. 2011 Small network test with 1 master and 2 RT PCs (done)
   - GE RFM, Dolphin RFM, DAQ, timing network
D. 2012-2013 Full test@ Kamioka new building
   - Constructing many RT rack modules

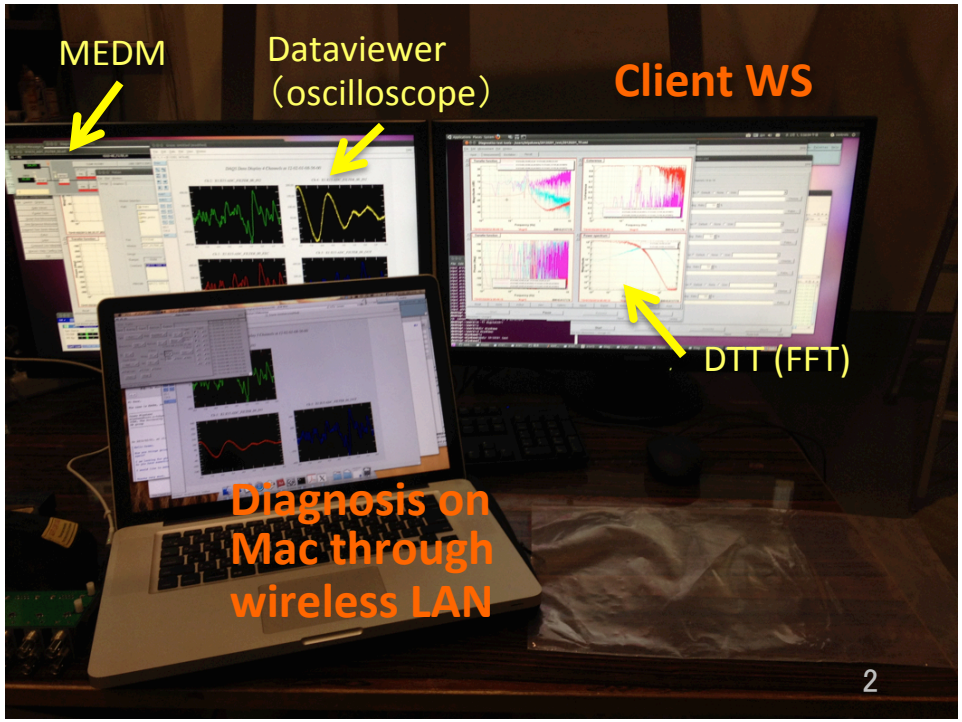


Installation into KAGRA mine

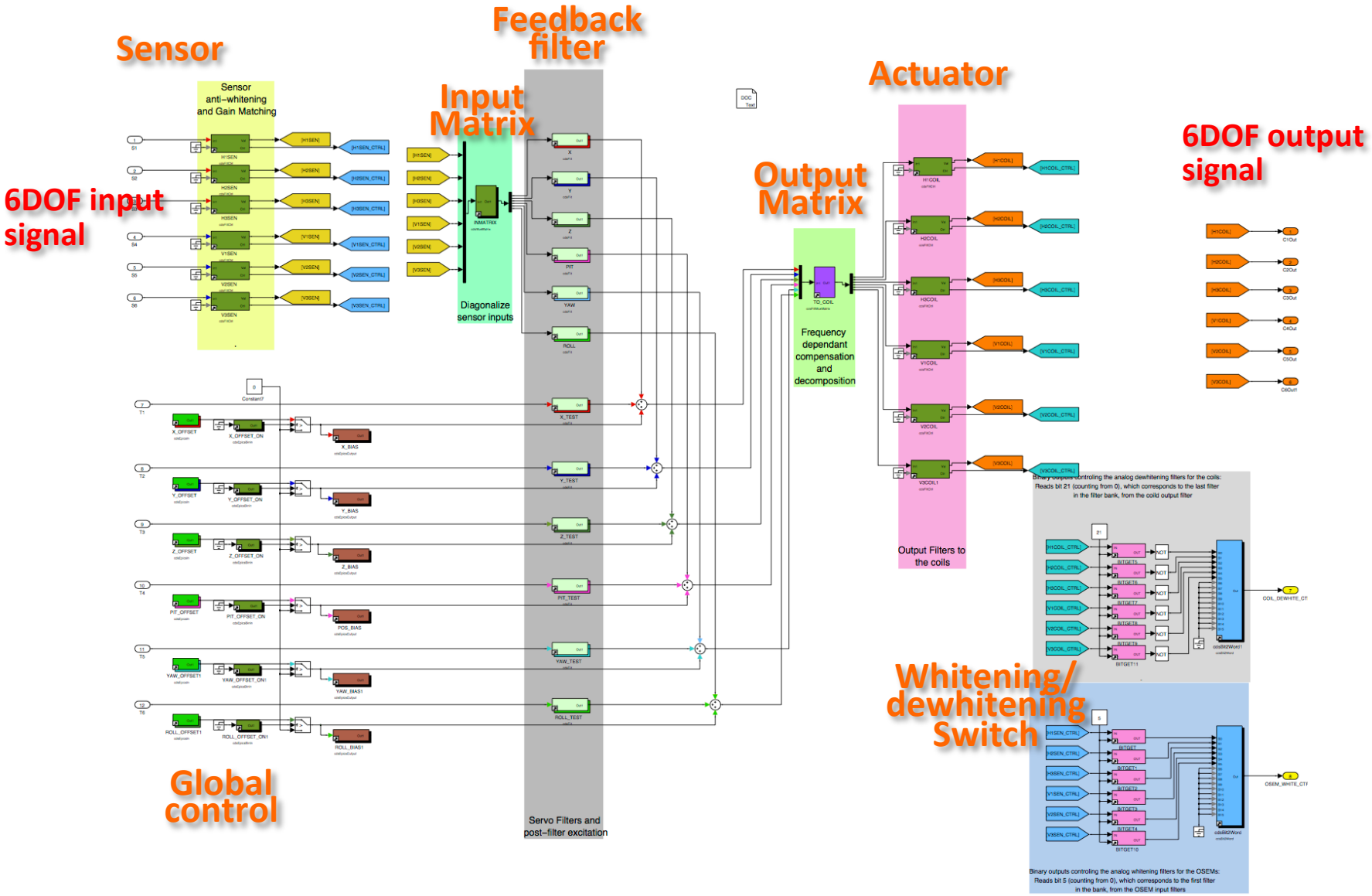
Delivering standalone digital system to VIS group at ICRR, Kashiwa



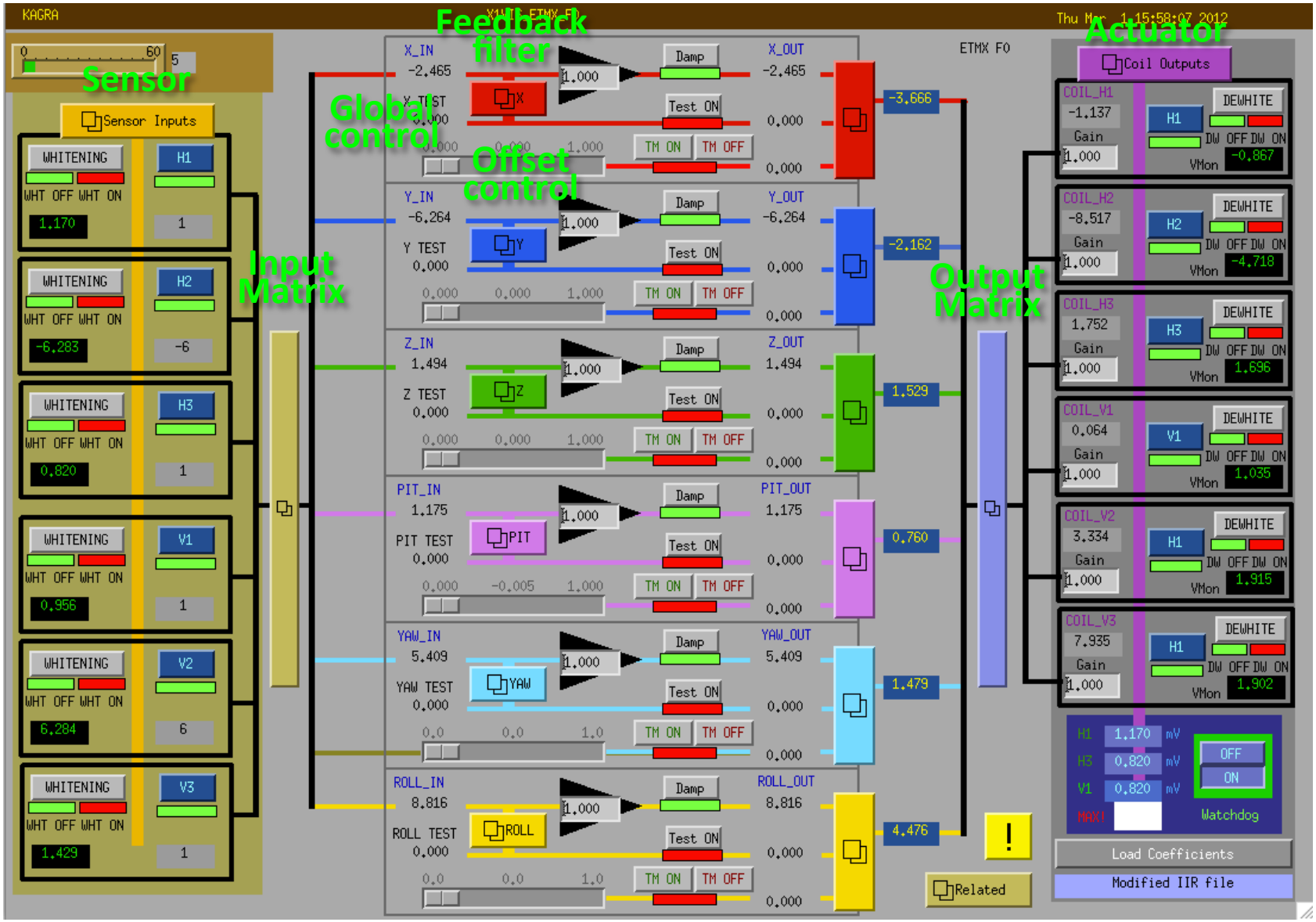
- Simple standalone system (RT PC + ADC/DAC, AA/AI, Client WS, router) has been delivered to VIS group at Kashiwa on 1/30/2012.
- 3days work for installation, lecture, training and measurement/control



Real time model for Pre-Isolator



MEMD screen -- GUI for EPICS --

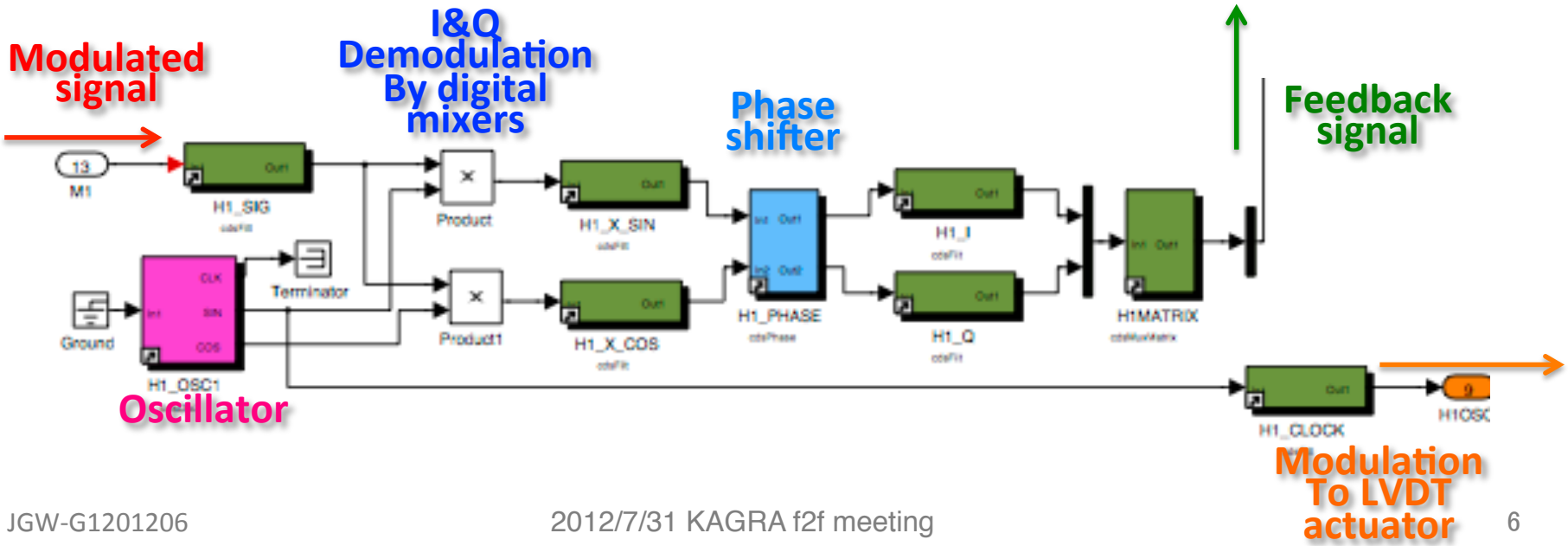



KAGRA
X1VIS_ETMX_F0_INPUT
Thu Mar 22 15:07:43 2012
CLEAR HISTORY
LOAD COEFFICIENTS
HOLD OUTPUT
DECIMATION
LIMIT
ON/OFF
OFFSET
FM1
FM2
FM3
FM4
FM5
OUT16
OUTPUT
KAGRA
X1VIS_ETMX_F0_X
X1VIS ETMX F0
X1 - VIS
X1VIS-F0_TO_COIL_1_1
Thu Mar 22 15:31:07
FM6
FM7
FM8
FM9
FM10
Ramp Time (sec):
OUTMON
H2
H3
V1
V2
V3
DEWHITE
Watchdog

A digital LVDT driver

Trial:

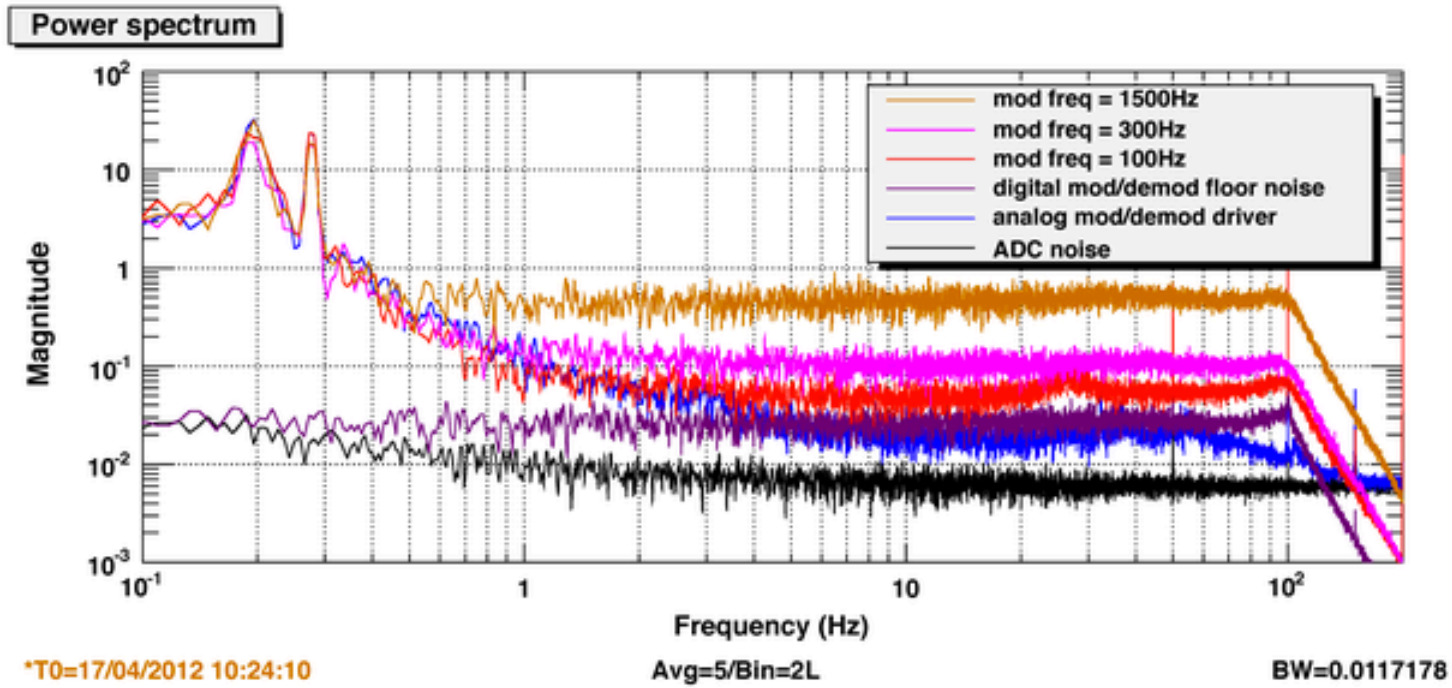
Replacing analog modulation-demodulation process to digital modulation-demodulation



A digital LVDT driver

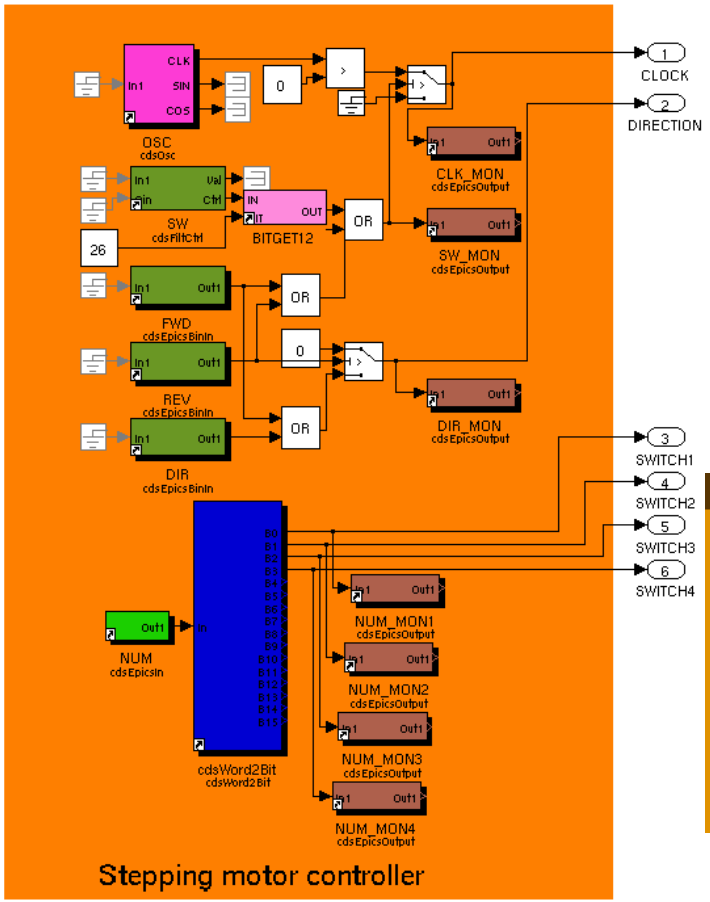
Result:

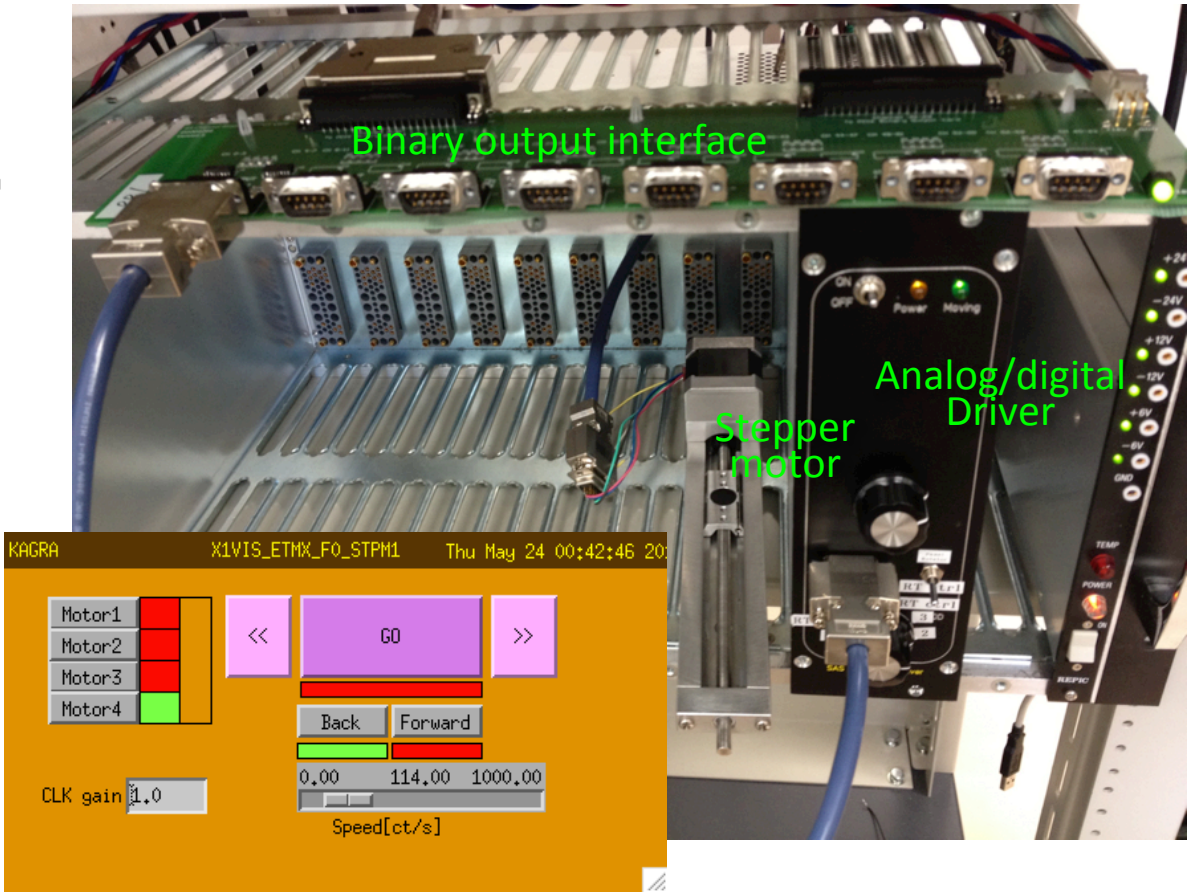
- Factor x3~4 worse than analog mod-demod process
- Lower modulation frequency was better, best:~100Hz
- Limited effective band-width up to ~ few Hz (actually being used only below 1Hz)
- Useful as temporary porpose
- Decided to keep ADC/DAC channels remaining for digital LCVDT driver



Stepper motor controller using Binary output

RT model





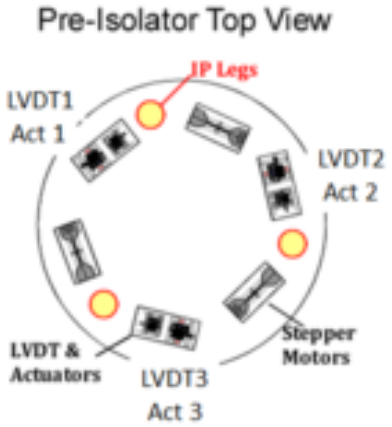
MEDM

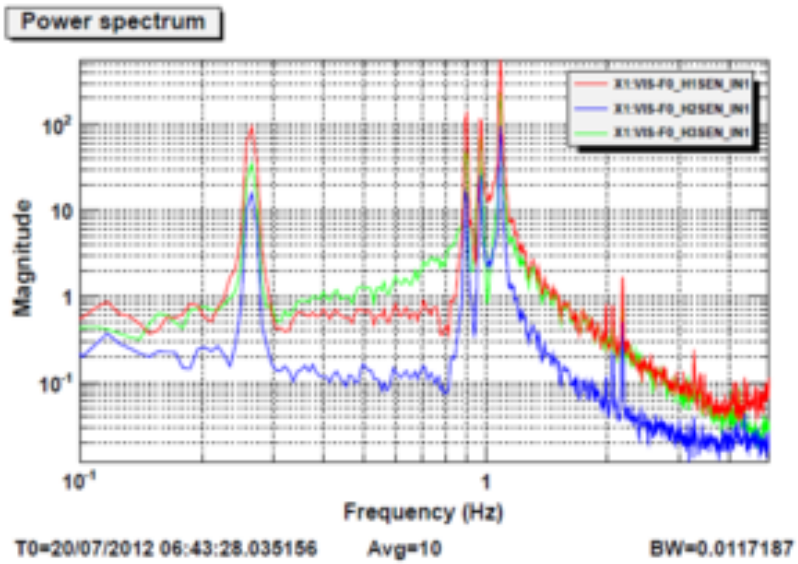
- Controlling up to 4 stepper motors
- 2bits for clock and direction
- 4 bits for switching 4 motors exclusively
- Servo script written in python

Installed into Pre-isolator at Kashiwa in June.

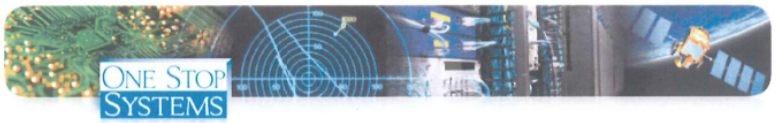
Instructions, troubles and recovers

- Preparing manual for user applications on Wiki.
- Instructions by e-mail when questions or troubles happened.
  - Long time data
- 1DOF (1 ADC channel / 1 DAC channel) test
  - Data full on 1TB HDD
    - needed to delete old data manually
  - No real time core running
    - A starting script was deleted somehow. Needed rebuild the model to reproduce the script.
  - Stepper motor driver trouble
    - Capacitance shorted, due to very old driver in TAMA era
- Multiple channel tests are being performed.
- We need more tests and more feedbacks from subsystem, but no other chance except for VIS! Please give us more chance to connect actual plants.
- Simulated plant



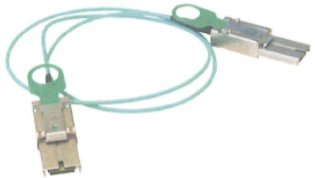


Development for Remote IO chassis



PCIe x4 Active Optic Cable

Fiber optic cable with PCIe x4 connectors.
OSS-PCIe-CBL-ACT-x4-10M
OSS-PCIe-CBL-ACT-x4-100M



Available in 10m and 100m lengths

PCI-SIG PCI Express Cable Specification Compliant

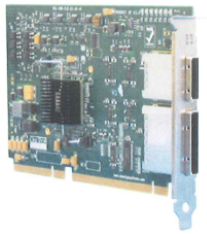
Positive latching mechanism per the PCI-SIG specification

TECHNICAL SPECIFICATIONS

PCIe x4 Active Optic Cable	
Cable Length	10m, 100m
Data Transfer Rates	PCIe Gen 1 – 10Gb/s PCIe Gen 2 – 20Gb/s PCIe Gen 3 – 32Gb/s
Gender	Male-Male
Temperature Range	Case operating 0° to 70°C
Lock to Mating Part	Yes
Fiber Cable Diameter	3.0mm
Wire/Cable Type	Round

PCIe x4/x8 Gen 2 Expansion Board

PCIe x8 or x4 Gen 2 expansion link board installs in SHBe slot of a PCIe Gen 2 backplane, allowing either x8 or x4 cable inputs from upstream host system.
OSS-SHB-ELB-x4/x8-2.0



- Can use either PCIe x4 and x8 cables
- Switch puts out PCI Express 20 lanes to backplane
- Lanes are auto configurable to backplane or can be user configured
- Lane active LEDs on slot cover
- Power acceptable LEDs on board

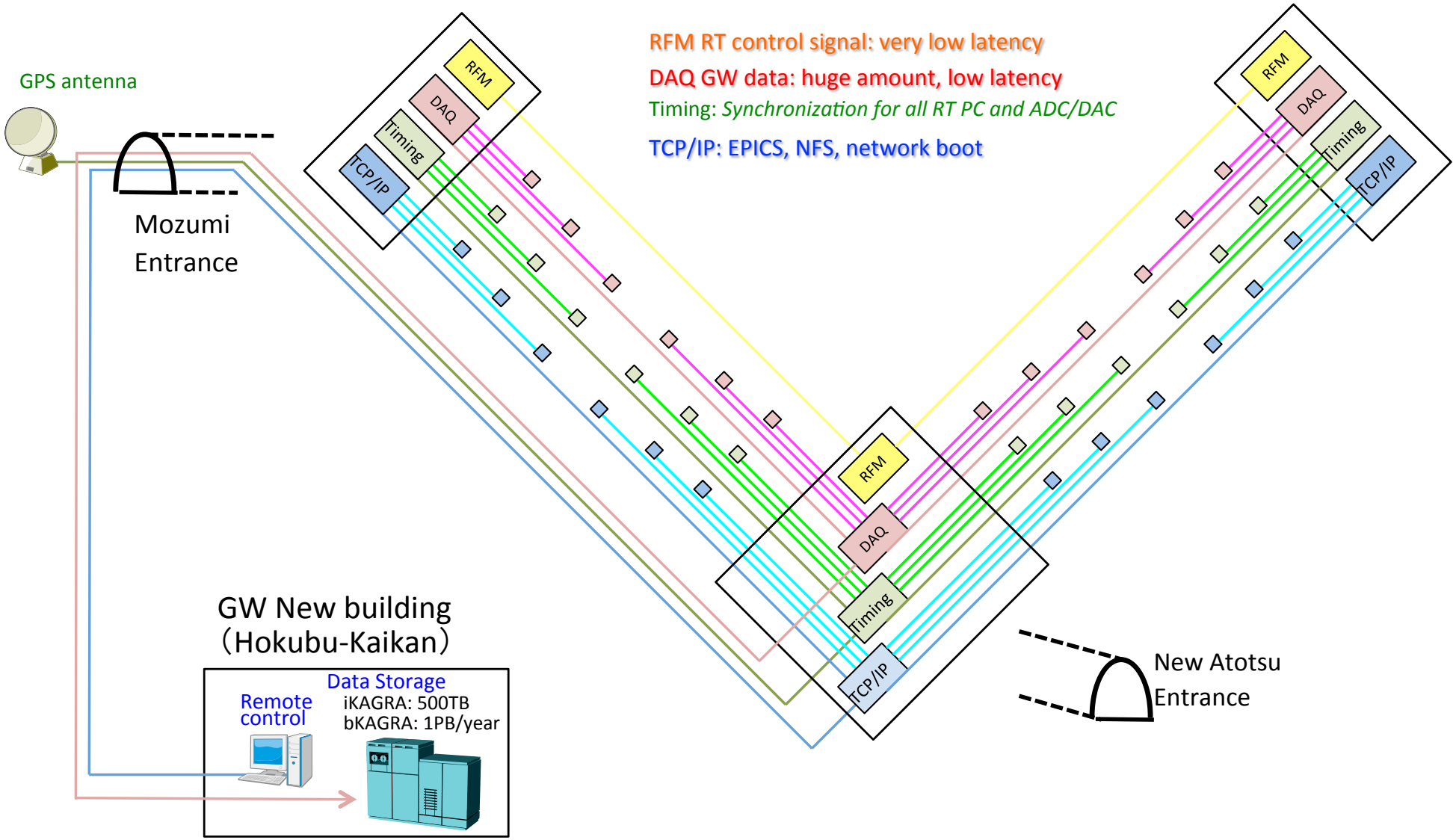
TECHNICAL SPECIFICATIONS

PCIe x4/x8 Expansion Link Board	
Form Factor	PICMG 1.3 SHB Express system slot compliant
Slot Type	System slot for the expansion chassis
Dimensions (H x L)	4.375 x 6.6 in (111 x 161 mm) 1 slot wide
Switch	PLX PEX8632 32 lane switch
Upstream Interface	PCIe x4 over cable, PCIe x8 over cable
Downstream Interface	20 lanes of PCI Express can be auto-configured as: One x16 and one x4 PCIe link, Two x8 and one x4 PCIe links, or five x4 PCIe links
Front Panel Connectors	1 PCIe x4 cable connector, 1 PCIe x8 cable connector
Front Panel Indicators	1 green LED for x4, 1 green LED for x8
Internal Indicators	Power In-range Indicators for +.2V, +3.3V & VTT (Red/Green), Power on indicator for +1V (Green), Bank of 5 board status indicators (Red)
Optional Features	Heat Sink: On-board fan header provided for optional heat sink fan
Temperature	0° to 50°C (32° to 122°F) default 0° to 70°C (32° to 158°F) with optional fan heat sink
Storage Temperature	-40° to 85°C (-40° to 185°F)
Operating Humidity	10 to 90% non-condensing
Storage Humidity	5 to 95% non-condensing
Shock	30g acceleration peak (11ms pulse)
Vibration	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration
Power Consumption	9W typical, 11.4W max, +12V @ 0.675A max, 3.3V @ 1.0A Max, 5V aux @ 2.5mA max
Agency Compliance	Designed to meet: FCC Class B, CE, RoHS

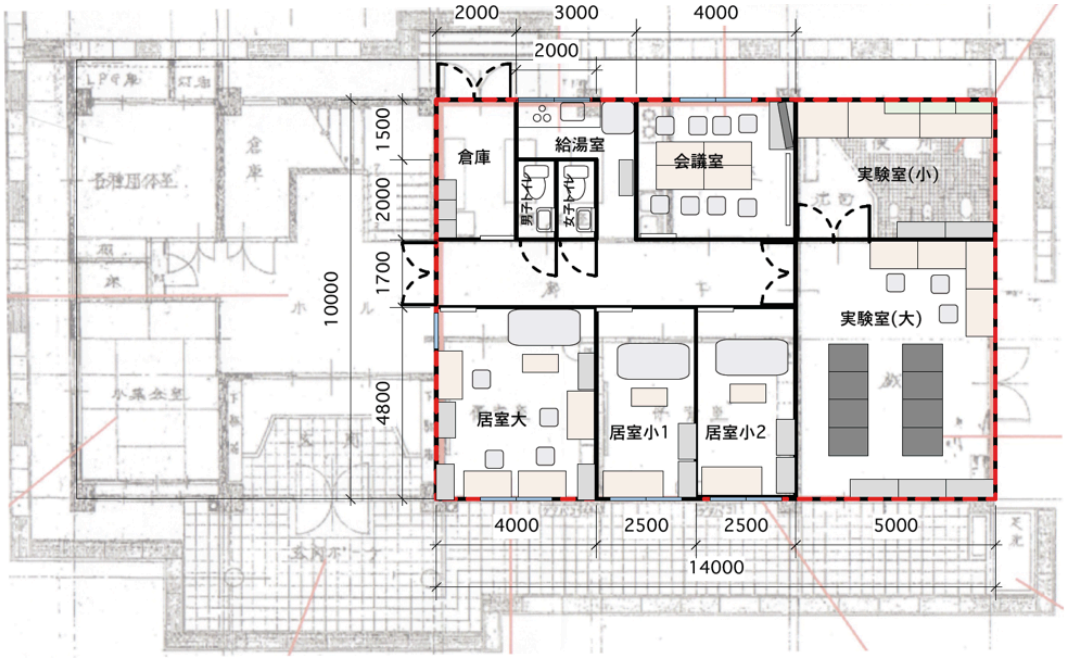
ONE STOP SYSTEMS

- No fan for calm environment
- Development and test with 6 prototypes in FY2012

Network design

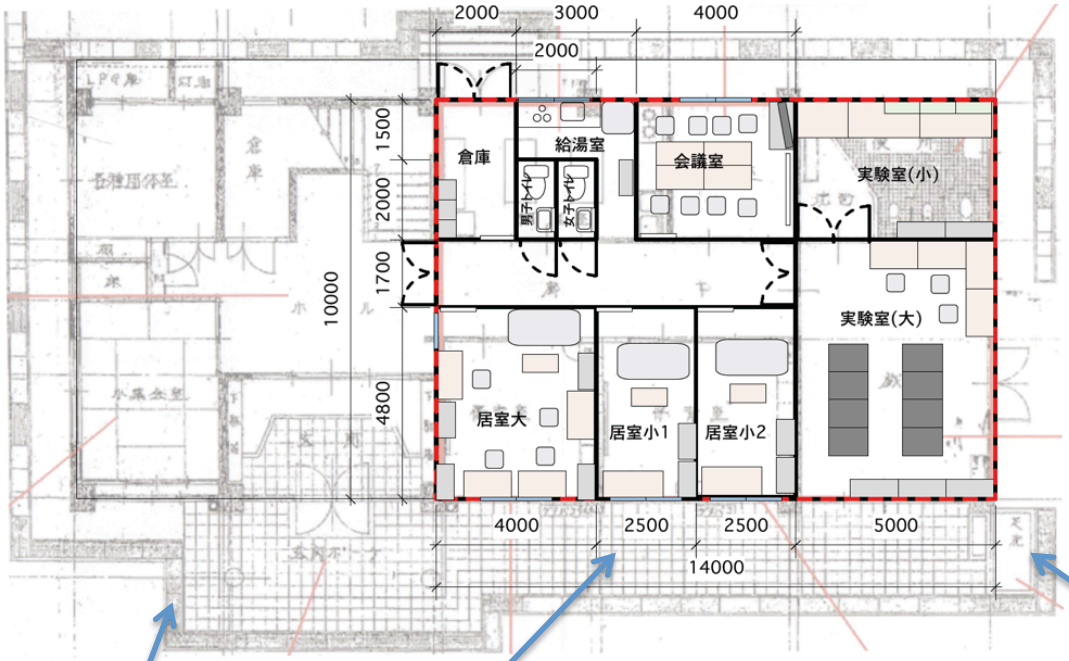


Hokubu-Kaikan

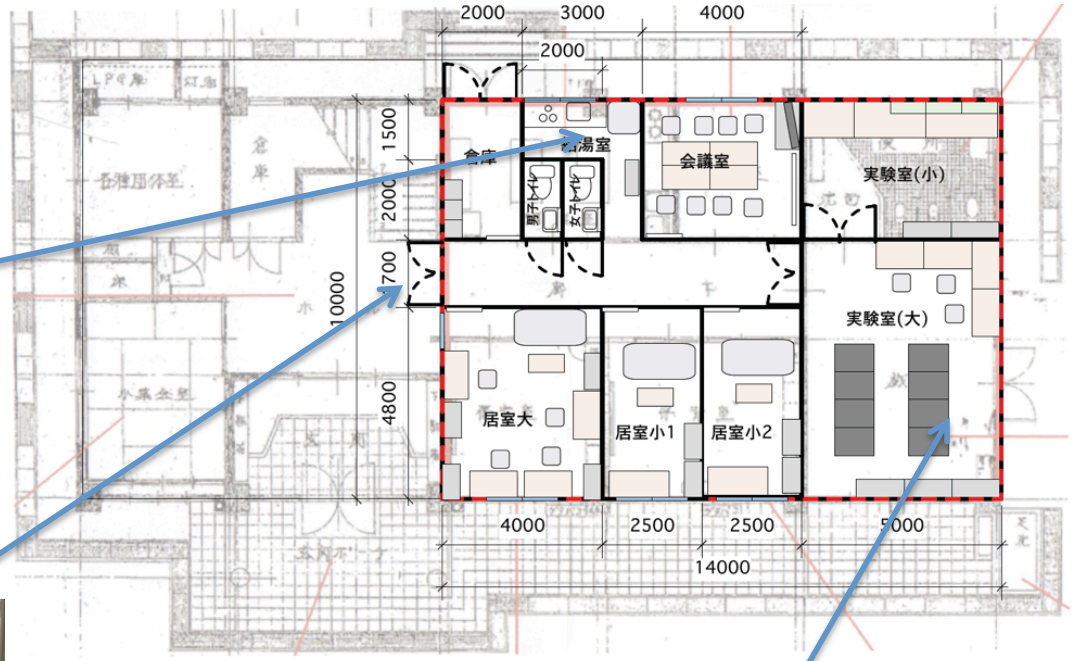


- Construction to be completed by end of July
- Inspection at Aug. 7
- Network connection in September
- Large experimental room for full Network test with digital control system
  - Redundancy, cyber security
- Small experimental room for electronics
- Capable for 6 residents

Hokubu-Kaikan



Hokubu-Kaikan



Recent work

- Making a signal list at ADC and DAC
  - To estimate more accurate No. of ADC, DAC, IO chassis and RT-PC
  - ~half of VIS and IFO transmitted ports are done
  - Listed ~900ch/3200ch
  - Current channel list: **JGW-T1201105-v3**
  - Next target: MIF and CRY
- Making a location list for ADC, DAC, IO chassis and RT-PC on 19 inch racks
  - Current list: **JGW-T1201168-v1**
- Lack of PCIe slots due to too many whitening switch
  - Slow BO?
  - Additional commercial IO chassis?

Resource list

RT PC Name	RT PC room	Roon No.	rack	IO chassi room	Room No.	rack	RFM	Dolphin	ADC	DAC	18bit DAC	BO card	BO cards for wh.	Total cards	AA	AI	whitening	BO ch. for whitening	BO for what	Items	Comments
k1ioo1	?	?		FMC-Area	9			1	4	2		1	8	15	4	2	8	29	OL x8, SS x4, ASC x16, MCL x1	MCI+MCO, (MCR, WFS2), PSL(PMC, FSS, ISS)	
k1ioo2	?	?		EMC-Area	10			1	2	1		1	2	6	2	1	2	6	OL x4, SS x2	MCE, (MCT)	
k1ioo3	?	?		FMC-Area	9			0	3	3		1	8	15	3	3	8	30	OL x8, SS x2, ASC x16, REFL x4	FI+MMT2, (REFL, WFS2)	
k1ifo1	?	?		P-Area	7			1	5	5		4	5	19	5	5	5	20	OL x12, SS x6, POY x2	PRM+MMT1?, PR3, (POY)	
k1ifo2	?	?		B-Area	4			1	4	4		4	9	21	4	4	9	36	OL x8, SS x4, ASC x16, POP x6, GRX x2	BS, PR2, (POP, GRX, WFS2)	
k1ifo3	?	?		B-Area	4			1	3	2		4	2	11	3	2	2	8	OL x4, SS x2, GRY x2	SR2, (GRY)	
k1ifo4	?	?		S-Area	5			1	5	5		4	8	22	5	5	8	30	OL x8, SS x2, ASC x16, POX x4	SRM+OMMT2?, SR3, (POX)	
k1omc	?	?		S-Area	5			1	?	?		1	9	10	?	?	9	35	OL x12, SS x2, ASC x16, ASRF x4, ASDC x1	OMC+OMMT1+OFI?, (ASRF, ASDC, WFS2)	
k1ix1	FrontVIPre (FrontMec)	41(24)		XFrontVI (XFrontCryoBack)	40(22)			1	2	3		1	2	8	2	3	2	6	OL x4, SS x2	ITMX	for Type A & C
k1iy1	FrontVIPre (FrontMec)	41(25)		YFrontVI (YFrontCryoBack)	44(32)			1	2	3		1	2	8	2	3	2	6	OL x4, SS x2	ITMY	for Type A & C
k1ex1	XEndVIPre (XEndMec)	61(54)		XEndVI (XEndCryoARsideDuct)	60(51)		1		3	3		2	8	16	3	3	8	30	OL x4, SS x2, TRX x24	ETMX, (TRX)	for Type A & C
k1ey1	YEndVIPre (YEndMec)	81(74)		YEndVI (YEndCryoARsideDuct)	80(71)		1		3	3		2	8	16	3	3	8	30	OL x4, SS x2, TRY x24	ETMY, (TRY)	for Type A & C
k1isc	C Control	1		?	?		1	1	2	0		0	0	2	2	0	0	0			
k1aux	C Control	1		?	?				2	0		?	0	2	2	0	0			AOS, PEM	
k1ix2	FrontMec	24		XFrontVI	40				5	0		0	0	5	1	0	0			low temperature, PEM	All EPICS channnel
k1px1	排気装置拡幅	?		排気装置拡幅	?				1	0		0	0	1	1	0	0			PEM	All EPICS channnel
k1px2	地震計拡幅	?		地震計拡幅	?				1	0		0	0	1	1	0	0			PEM	All EPICS channnel
k1px3	XGeoEnd	91		XGeoEnd	91				1	0		0	0	1	1	0	0			PEM	All EPICS channnel
k1ex2	XEndMec	54		XEndVI	60				5	0		0	0	5	1	0	0			low temperature, PEM	All EPICS channnel
k1iy2	FrontMec	24		YFrontVI	44				5	0		0	0	5	1	0	0			low temperature, PEM	All EPICS channnel
k1py1	排気装置拡幅	?		排気装置拡幅	?				1	0		0	0	1	1	0	0			PEM	All EPICS channnel
k1py2	地震計拡幅	?		地震計拡幅	?				1	0		0	0	1	1	0	0			PEM	All EPICS channnel
k1py3	YGeoEnd	96		YGeoEnd	54				1	0		0	0	1	1	0	0			PEM	All EPICS channnel
k1ey2	YEndMec	74		YEndVI	74				5	0		0	0	5	1	0	0			low temperature, PEM	All EPICS channnel
						Total	3	10	66	34		26	71	197	50	34	71	266			

- 20-24 RT-PC
- ADC/DAC/BO enough? but limited budget.

Channel number

- Asking CRY group to reduce channel numbers for temperature monitor
- Request from CRY: total number 424ch for 4 cryostat -> 16ADC
  - Cost: $4000 / 32ch ADC + $4500 / 32ch AA filter
- Request of DGS: 64 x 4 = 252ch for 4 cryostat -> 8 ADC
  - Maybe reduces the number of RT PC
  - Cost: (RT PC $5000 + IO chassis $13000) x 4 = $72000

- Not difficult to increase channel numbers when another budget available in the future.

Analog electronics

- Asking several companies for mass production of electronics
  1. Design boards -> each subsystem
  2. Making boards, soldering electronic parts
  3. Making chassis
  4. Putting them into chassis
  5. Inspection -> limited test due to technological difficulty, limited budget
- Making an electronics list with existing diagram (ex. LIGO DCC)
- Lecture soon!
  - How to order analog electronics to AEL subgroup