Document of Digital System Subgroup for 2nd External Review

JGW-T1200910

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Digital system subgroup members

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1. Overview

1-1. Definition and scope of the subsystem

Digital system (DGS) subgroup is in charge of development of a whole real time control system for a km scale interferometer with flexible human interfaces. This system has the functions which digitalize analog sensing signals extracted from the interferometer and each subsystem, and produce signals in the computer for controls, monitors, switches and diagnoses, and re-produce analog signals to actuate the interferometer.

This subsystem has following items.

I. Development of real-time (RT) control computer
   (a) Signal input/output using ADC/DAC modules
   (b) Binary switch using binary output (BO) modules
   (c) Real-Time core software
   (d) Real-time communication network interface
II. Development of client workstations including monitor/diagnosis software
III. Network design and development for following data transfers
   (a) Real time control network
   (b) Timing network
   (c) Data acquisition (DAQ) network
   (d) General network
IV. Producing frame data for data storage/analysis

1-2. Important interface

Important interface between each subsystem and our DGS is listed as follows.

- FCL: network infrastructure, isolated room, entrance/exit system, monitors in control room
- VAC: vacuum monitor, Gate valve switch
  -> channel list, connector shape, EPICS interface
- VIS: OSEM, oplev, stepper/pico motor
  -> channel list, connector shape, variable gain amp, whitening/dewhitening,

stepper/pico motor driver

- CRY: temperature monitor, switch for cryostat
  -> channel list, connector shape, EPICS interface
- MIF: IFO control for LSC and ASC, switch for common mode servo, tuning, diagnostic, auto lock, auto alignment, calibration, online monitor, operation, observation
  -> channel list, connector shape
- AEL: PD signal (DC), QPD signal (DC), I & Q servo output signal, switches for circuits, DC power supply monitor, DC power supply, cable, connector, AA/AI filter, VGA, whitening/dewhitening
  -> channel list, connector shape
- IOO: switch for for PMC, FSS, MC, OMC servo, FSS temp. control, control for MC and OMC, modulation depth controller, pico motor for steering mirror, pico motor for circulator
  -> channel list, connector shape, pico motor driver
- LAS: power/temperature monitor, thermal control, inter lock
  -> channel list, connector shape, EPICS interface
- GIF: physical environment monitor
  -> channel list, connector shape
- DAT: frame data, online analysis, calibration, data rate
- AUX: Oplev, picomotor for steering mirror, CCD monitor switch
  -> channel list, connector shape, EPICS interface

Digital system subgroup provides a platform to realize above functions. The concrete function should be implemented by each subgroup by developing interface driver or the software. We ask each subgroup to develop application software like real-time interferometer control model, data analysis software using frame data and so on. We offer typical example for real time models or GUI interfaces, and we also offer instructions/lectures for how to use the digital system.

1-3. Design phase

1-3-1. Slow EPICS network:

KAGRA uses many stepping/pico motors. They are sometimes in a control servo for

example local damping control in seismic isolation. Slow EPICS control might be used for the control of such motors. Currently New Focus PicoMotors are able to be controlled on EPICS with a standalone digital system, but other kind of motors should be supported and they should work in the whole KAGRA network through the 3km arms. Slow EPICS network is still at the very preliminary design phase.

1-3-2. Simulated Plant:

Simulated Plant using digital system is a testing tool the control performance of subsystem when constructions of subsystem are in progress or even when materials do not exist in the design phase. Real-time control codes can be built and the attached scripts etc. can be tested independently outside of the mine, and it can be combined when the real materials are constructed. We are in progress to develop the simulated Plant. It will be very useful for KAGRA construction since the working time in the mine will be limited.

2. iKAGRA

2-1. Target specifications

2-1-1. Requirements

We aimed to satisfy following parameters for the km scale interferometer to detect gravitational waves (GW);

A) Observation bandwidth >5kHz
B) Dynamic range >120dB
C) Control bandwidth >200Hz
D) Number of channels >1024
E) Number of output channels >256

Required dynamic range is determined by the amplitude and noise of error signals of interferometer during GW observation, or by how much dynamic range the lock acquisition needs. Reason for this 120dB is explained in Appendix A.

To satisfy this requirement, we define our internal requirements in Table 1. We selected

16bit ADC/DAC for the required dynamic range. From this table, the dynamic range of ADC will be >15V/3uV=134dB and the dynamic range of ADC will be > 10Vpp/3uV = 130dB.

Item	Requirements	Comment
Sampling rate	>=16384Hz	65536Hz at ADC, then decimated to 16384Hz
ADC bit resolution	>=16bit	
Dynamic range of input	>=+/-15V	Differential input
Dynamic range of output	>=+/-10V	Differential output
ADC noise	<3uV/rHz	Effectively reduced by whitening filter
DAC noise	<3uV/rHz	Effectively reduced by dewhitening filter
time delay	<100usec	For >200Hz UGF
Input channel numbers	>2048ch	(16kHz:>128ch, 2kzHz:>512ch, 64Hz>1024ch)
Output channel numbers	>512ch	For mirrors, seismic attenuators, PZTs etc.
Stored channel numbers	16kHz:>64ch, 2kzHz:>512ch, 64Hz>1024ch, 16Hz>10000ch	~300TB/year

Table 1. Requirements for digital subsystem

2-1-2. Hardware

Real-time Core (RTC) runs on computers with the following minimum configuration:

1) Dual x86 processors, with four CPU cores each.
2) Processor clock speed of 3GHz.
3) Eight (8) Gigabyte of memory.
4) Two Gigabit Ethernet interfaces.
5) One, or more, real-time network interfaces
    a. Reflected Memory (RFM)
    b. PCI Express (PCIe) network interface

6) A PCIe interface to the PCIe expansion chassis with a maximum of 10 PCIe cards installed.

2-1-3. Software

The software is divided into the following functional groups;

I. RTC Software:
   (a) Real-time Sequencer (RTS): That software which performs the functions of scheduling and I/O interfaces for all real-time applications.
   (b) DAQ: That software which performs the function of real-time data acquisition and data formatting.

II. Real-time Common Library: A standard real-time code library for use in all real-time user applications.

III. Real-time Support Software: The software necessary to communicate between the RTC and operational support and DAQ software via Ethernet connections. This includes:
   (a) EPICS interface software
   (b) Arbitrary wave form generator (AWG) / Test point manager (TPM)
   (c) DAQ Network Interface

IV. Real-time System Monitor: Software to run on a designated real-time computer designed to monitor the overall status of all real-time systems and networks.

2-2 Final design

2-2-1. Network design

Design of network for digital system is equivalent to the design of whole network of KAGRA in mine. We listed up necessary networks here;

I. Real-time control network: connection during RT computers for control
   (a) GE Reflective memory network (RFM)
      Hub: GE Fanuc 5595
      Cable: single mode fiber, <10km
   (b) Dolphin Reflective memory network
      Hub: Dolphin DXS410

Cable: metal or fiber, x10 faster than GE RFM, <100m

The most important network is a network for the real-time control signals that are transmitted trough the reflective memory (RFM). Amount of the real-time control signal is not so much, but must be enough fast to avoid any lose of locking. RFM technology assures a very low latency even for the km long scale.

II. DAQ network: data collection stream from all RT control computers to raw data storage

Router: NETGEAR 7224/7352, Fujitsu XG2600 or similar

Protocol: OpenMX for each RT PCs and Myrinet(10GigE) for data concentrator

Cable: metal (CAT6 or 7) between PCs and a router, 10GigE fiber among routers

Amount of GW data will huge like ~1PB/year, so we need quite enough band-width for the GW data network. GW data won't require so strict low latency like control signal, but time information will be stamped to the GW data, so we require some low latency for the data transfer limited by angular resolution of direction of GW source. For such reasons we employ Myrinet protocol that has lower latency than TCP/IP.

III. General network: PXE network boot for RT control computers, client workstations for control/monitor/diagnosis in control room, security and authentication, EPICS, NAT, NTP, NFS, blog, wiki etc.

Router: NETGEAR 7224/7248 or similar

Cable: metal (CAT5e or 6) between PCs and a router, 1GigE fiber among routers

This whole network design includes a general network in KAGRA like web browsing or e-mail and so on because human interfaces for control of KAGRA uses EPICS and the EPICS runs on the general TCP/IP network.

IV. Timing network: timing distribution system (TDS) of absolute time for all RT control computers, and 1PPS signal for ADCs/DACs

GPS antenna, Master/Fanout/Slave timing system designed by aLIGO

Other important network is a timing signal distribution. All ADC and DAC even apart 3km away must be synchronized for real time control. We use Master-Slave timing system developed by aLIGO with corporations of Columbia University. This system provides a proper timing compensation for a delay between Master-Slave or Master-Fanout by km scale long distance. It is suitable for us that a GPS antenna will be located out of the mine and a Master timing chassis will be located near the antenna, then the timing signal from the Master will be transmitted into the KAGRA mine and reach to a Fanout chassis at the vertex. Fanout chassis is similar to Master chassis, but has no GPS receiver inside. It is the same as Master that Fanout has multiple output ports of timing signal to Slave boards. Fanout will be located at each end room and the timing signal between the vertex and the end will be connected by Fantou-Fanout.

A simple schematic of RFM, DAQ and general network is shown in Fig. 1, and a simple schematic of timing network is shown in Fig. 2. Detailed diagram for all network connection are drawn in in JGW-T1200791.

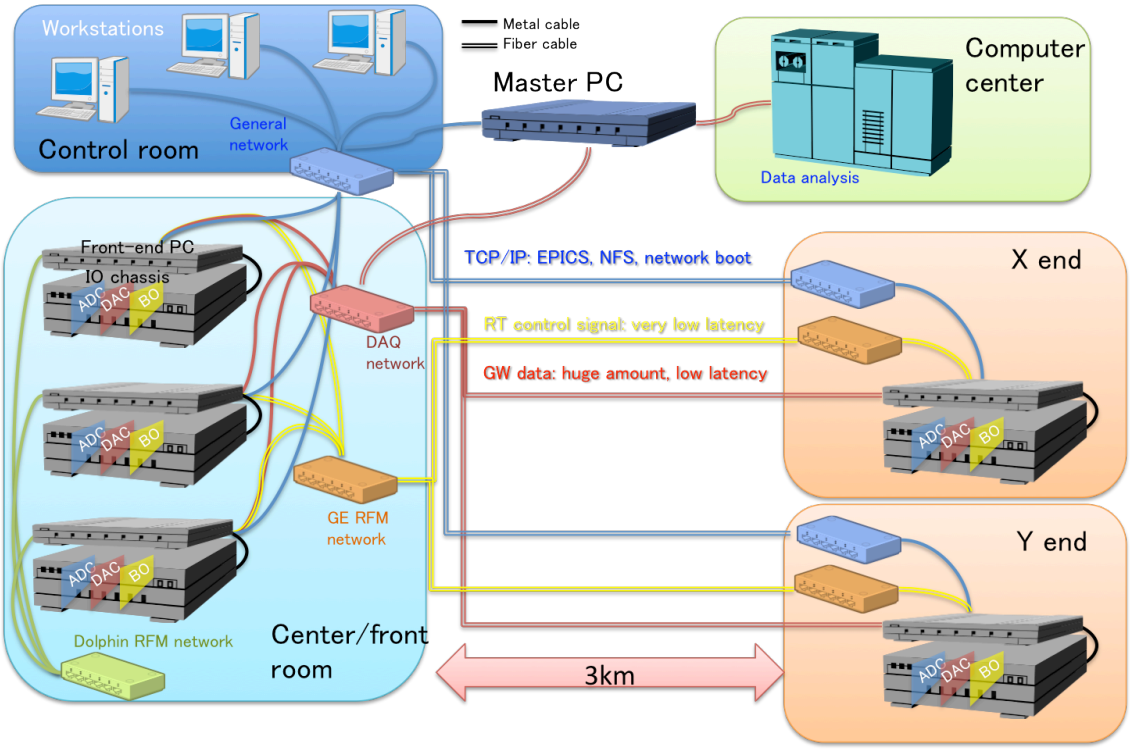

Figure 1. Conceptual connection diagram for whole KAGRA network

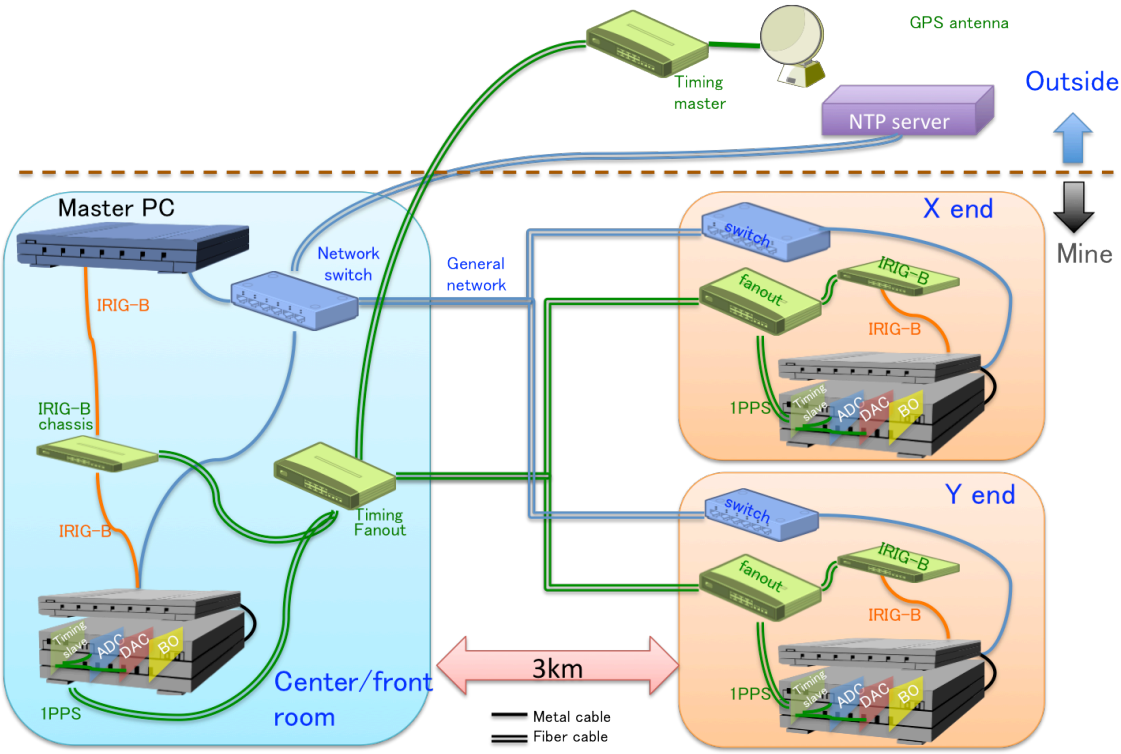

Figure 2. Conceptual connection diagram for timing network of KAGRA

2-2-2. Interface

Interface for signals

Our main interface to other subgroups is for the signal input/output and switch. These interfaces are defined as follows;

Signal input

- ADC 32ch/card, differential (64ch for single input)
- Sampling rate: 16384Hz
- Maximum input range: +/-20V
- Noise: 2uV/rHz
- Input filter: Anti alias filter
- Connector: D-sub 9 or 37 pin (for differential 4ch)

Signal output

- DAC 16ch/card (32ch for single output)
- Maximum output range: +/-10V
- Noise: 1.5uV/rHz
- Output filter: Anti imaging filter
- Connector: D-sub 9 or 37 pin (for differential 4ch)

Switch

- Binary output (BO) 32ch/card
- Output voltage: 0 or +5V
- Connector: D-sub 9 or 37 pin (for differential 4ch)
  (Ex. Variable gain amp for 16 steps/1 D-sub connector)

Frame data

Digital system subgroup is responsible for data acquisition and data formatting. All KAGRA data will be formatted as the same as world standard GW data (like LIGO, VIRGO) through Frame Builder (FB). FB is a part of digital system and produces frame data with time stamp by timing synchronization system. Frame data will be stored through DAQ network into the raw data archive that is 100TB class RAID data storage located at the front room in the mine. This raw data archive is a temporary data storage that can be used for commissioning or pre-data analysis at the local site. Stored data should stay at the local site for longer than 1 month. Simultaneously the stored data will be sent to another Peta-Byte class huge data storage that will be placed at Kamioka-building or Kashiwa GW computer center (to be determined). This huge storage will be prepared by data analysis subgroup.

Data transfer rate

Data transfer rate can be estimated the number of DAQ channels. The number of channels is not determined yet, so we assume following channels shown in the list;

	Number of stored channels	Float 16kHz:128ch Float 2kHz:512ch Float 256Hz:1024ch Float 16Hz:65536 epics channels
	Data transfer rate	8MB/sec for 16kHz

		4MB/sec for 2kHz 1MB/sec for 256Hz 6MB/sec for 16Hz Total ~20MB/sec (~70GB/hour, ~2TB/day ~600TB/year)

2-2-3. Related analog circuits

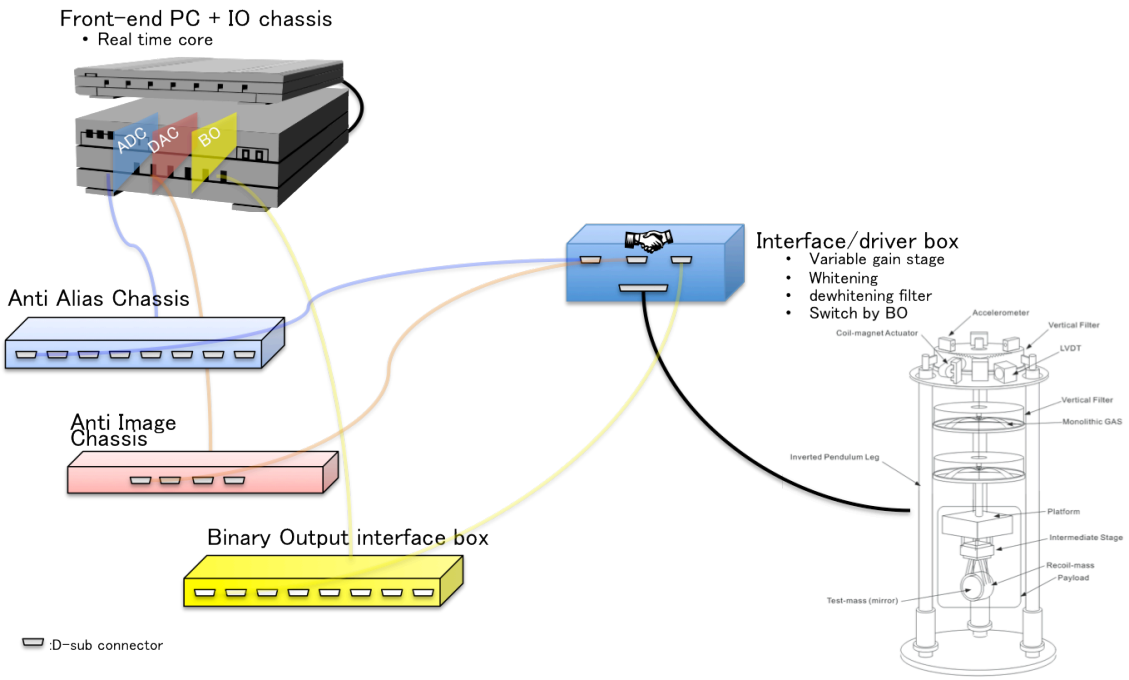

Figure 3. Typical connection between digital system and subsystems

Conceptual diagram for connection between digital system and subsystems is shown in Fig. 3. Typical signal stream will be like following order;

I. Analog signal -> satellite box (including variable gain amplifier (VGA), whitening filter (WF)) -> long metal cable (~10m) -> driver box ->
II. AA filter -> ADC-> Computer -> DAC -> AI filter ->
III. Driver box -> long metal cable (~10m) -> satellite box (including dewhitening filter (DWF)) -> actuation signal

Digital system subgroup is responsible for II of this stream. An anti alias (AA) filter is required for ADC input, and an anti imaging (AI) filter is required for DAC output to

avoid alias and image respectively. AA chassis and AI chassis are provided by digital system subgroup. AA and AI filter have the same frequency response that has a steep low-pass filter at the half of raw sampling frequency and notch filter at the sampling frequency (65536Hz).

On the other hand driver boxes or satellite boxes should be manufactured by each subgroup. Typical circuit diagram will be offered from DGS subgroup.

Typical whitening/dewhitening filter has zero-pole/pole-zero for 15Hz and 150Hz or near around these frequencies. These frequencies will be tuned for each target subsystem. Variable gain amplifiers (VGA) should be also implemented upstream whitening filter with several gain steps which will be controlled by BO signals. For example, 4bit (of 32bit of one BO module) can have 16 steps, so one BO card can control 4 VGA in this case.

2-2-4. Rack design and location

All RT control computers, circuits, network equipment are mounted into 19 inch rack. Total 20-30 (depending on the number of channels) RT racks will be located inside KAGRA (Fig. 4). Currently following racks are planned and categorized as

I. Red: Laser and input opics (1)
II. Blue: length (1), WFS (1), auxiliary (2)
III. Green: MC(1), PRM(1), SRM(1), MMT+BS(1), ITMX(1), ITMY(1), ETMX(1), ETMY(1)
IV. Purple: Physical Environmental Monitor (9)

Rack for Laser/IOO and racks for vertex suspensions will be surrounded by an isolated room located around MC.

Additionally racks for servers (black) are located in the front room. Server PCs consist of boot server, NFS, data concentrator, NDS, data storage etc. The number of racks will be ~5.

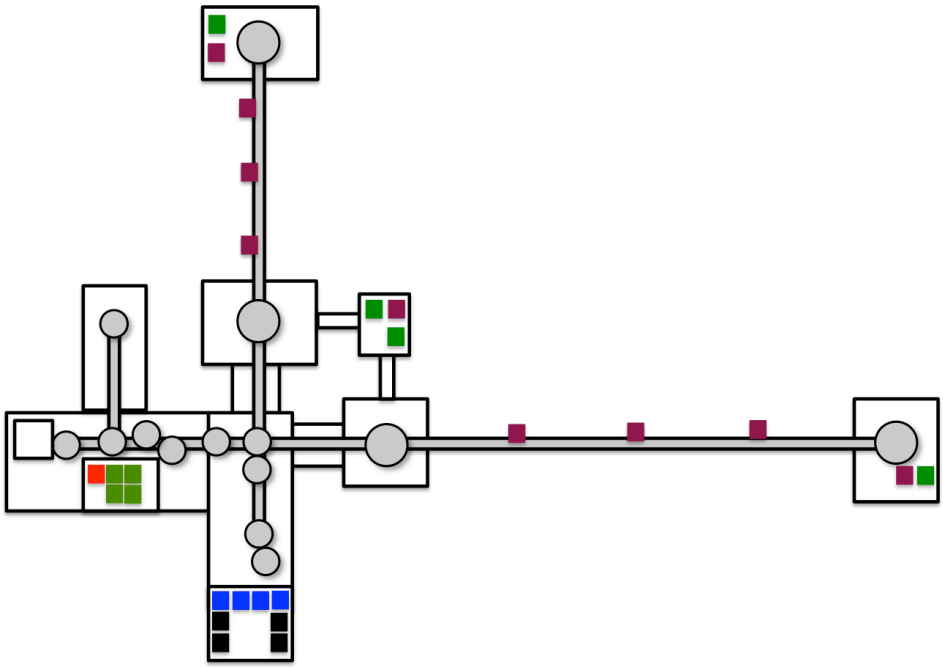

Figure 4. Location of racks for digital system.

2-3. Schedule

FY		2010				2011				2012				2013				2014				2015				2016			
Quarter		1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
Main Phase		Design								Tunnel								Vacuum				FPMI				RSE			
Prototype test	CLIO operation																												
	Data analysys test																												
Standalone system for subsystems	Hard/software setup																												
	Circuit																												
	Delivery																												
Article test	Small network																												
	Large network sytem																												
	Circuit																												
	Inspection																												
Full system	Installation																												
	Tuning																												
Upgrade	RSE																												
	Cryo																												

Table 2. Schedule of digital subsystem.

Current schedule is shown in Table 2 with 6 categories; prototype test, standalone system, article test, full system, upgrades. These stepwise developments assure the quality of system.

We started a prototype test for single RT PC at CLIO from 2009. The channel numbers

was not so many, but we tested basic functions for IFO operation like lock acquisition, calibration, noise performance check and so on. Details are explained in the next chapter.

Standalone (STDA) system for subsystems is based on experiences at CLIO prototype test and we expect many feedbacks from each subsystem.

As the next step, we will have a Small network connection test using 2 or 3 RT control computers. Real time control using a single computer is not so difficult, but if two or more computers are connected, real time control will be much more difficult due to network bandwidth, latency, synchronization etc. Currently (the end of FY2011) that test is done. This setup will be extended to a Large network system that has 7-10 server PCs and ~5 RT PCs. This would be a very important test as a full network operation to check enough network bandwidth and latency.

This Large network system will be moved into mine and it will be an actual full system for installation and tuning.

2-4. Quality assurance

2-4-1. Prototype Test Plan

Initial basic prototype test for digital system has been performed in Japan using CLIO 100m prototype interferometer in 2009-2010. It was a simple setup which has a single real time PC with CentOS + WindRiver Real time kernel as a classical aLIGO RT system, 1 ADC, 1 DAC, and 1 BO in a commercial IO chassis (One Stop Systems). Timing signal of 65536Hz square wave was injected from a general waveform generator. We designed prototype electronics for anti alias, anti image, BO interface. Also we needed single end to differential drivers since all the CLIO input/output was single ended. All PC, IO chassis, electronics are mounted into a 19" rack.

We tried following things;

- Setting up Real-time control computers
- Setting up client workstation with diagnostic software like dataviewer, DTT, MEDM
- Manufacturing analog electronics as AA/AI, BO interface.
- Lock acquisition
  - linearizing error signal
  - normalizing power

- Calibration process on DTT
  - sensitivity monitor
- Noise performance
  - switching whitening/dewhitening filters for signal by BO
- Auto lock acquisition operated with acquisition/down scripts
- Auto alignment using Python based Pico motor controllers on EPICS
- Application for other R&D experiment

We eventually succeeded in locking the mass control loop of CLIO and showed the performance that the noise of ADC and DAC was at least 10 times bellower than best sensitivity of CLIO for low temperature operation (shown Fig. 5). We also performed some application technics using the digital system like producing normalized error signals, auto alignment procedures, auto lock procedures and so on. This was a really good performance test for us leading to KAGRA because Japanese group has no or very limited experience for digital control system at that time.

During these experiences, we learned how to obtain required equipment to construct a digital system in Japan with a reasonable price and reasonable term. We are now thinking that there is no problem to use aLIGO type digital system in Japan for KAGRA.

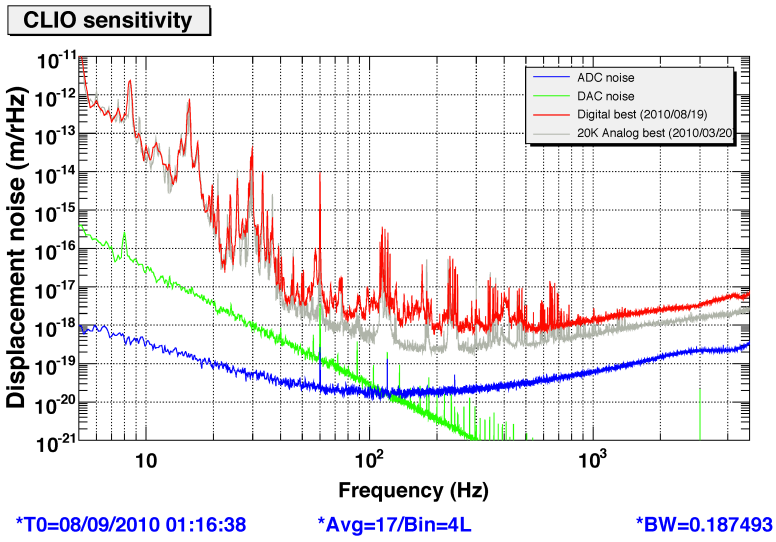

Figure 5. Calibrated CLIO displacement noise using digital system

2-4-2. Distribution standalone systems

The main prototype test is being performed from FY 2011 by delivering standalone (STDA) digital systems to other subgroups. Total 5sets of standalone digital system will be provided from DGS subgroup to other subgroups who need a digital system for development of their subsystems. Following items will be offered to subgroups;

1) Real-time control computer as front-end
2) Client workstation + monitors with some diagnostic software
3) PCIe I/O chassis
4) ADC, DAC, Binary Output
5) Anti Alias/Anti imaging filters

We will offer a typical RT model files and MEDM screens for each subsystem and we are planning some lectures or instructions to explain how to build a RT model and how to use diagnosis/control software. In FY2011, we delivered two STDAs. One is installed at NAOJ for a test bench of data analysis software using frame data and another one is for VIS group to investigate Pre-Isoator at IRCC Kashiwa campus.

This prototype test can provide good chances for each subgroup to be accustomed with a digital system before the commissioning of KAGRA starts. It is very important to extract the full performance of subsystem by using an actual digital system. We hope that new applications or technics will be invented from KAGRA's subgroup in not so far future.

2-4-2. Small/Large network test

We plan to have a test operation system with some RT computers and networks for a preparation of whole KAGRA network. This test has two steps.

The first step is the small-scale network test which has one master PC and two RT PC to investigate basic functions for important networks. Target networks are GE reflective memory, Dolphin reflective memory, DAQ network, timing network and general TCP/IP network. This test was performed at Kashiwa campus first with Joe Betzweiser who worked on Caltech 40m's CDS things, then move to Kamioka building. We have verified real time communication test between to RT PCs and DAQ data

transfer test from two RT PCs to Master PC with proper timing synchronization.
The second step is the large network test by extending the number of PCs from small network test to be closer setup to full KAGRA network. This will be placed in a new building that will be built in FY2012 near the current Kamioka building.
This system consists of following equipment as

1) ~5 RT computers with I/O chassis
2) ~2 client workstations
3) GPS antenna
4) Timing network with Master /slave timing board
5) DAQ network with 10GigE data transfer
6) GE RFM network for long distance
7) Dolphin RFM network for shot distance
8) EPICS network on 1GigE TÇP/IP network
9) Fiber connected network routers
10) Several network PCs (1 file server, 1 NTP server, 2 NDS servers, 2 data concentrator, 2 DAQ servers)
11) UPS for accidental power failure
12) Security and authentication system.

The first priority of this large scale test is for redundancy and security. Multiple computers for NDS, data concentrator and DAQs will be prepared for their redundancy with some security. Note that this setup does not care for actual signals including electronics like AA/AI. Manufacturing electronics will be discussed with AEL group.

2-5. Installation/Adjustment Procedure

Whole test system at the new Kamioka building will be moved into KAGRA mine when the installation of KAGRA starts after tunneling, by following the rack location plan shown in 2-2-4. Standalone systems that have been used by each subsystem will be merged into the whole KAGRA system. One of the advantages of distributing standalone systems is what the same RT models made in the standalone system can be used in the actual whole KAGRA system. It may extremely reduce the installation / tuning time for KAGRA.

RT PCs are setup with not hard disk and they can be network booted from boot server located at the front room, so an installation of additional RT PC is quite easy, by adding several lines at the boot server.

One of the concerns is that some subsystems start their installation without enough prototype tests and the connection to digital system happens when the actual installation started in KAGRA mine. We will prepare for a simulated plant for subsystem which can not be tested before installation, but basically all the subsystems should be tested with our digital system before the installation since time in the mine is very limited.

Actual installation will starts with some limited channel numbers for iKAGRA and the number of channel will grow for bKAGRA, but essentially there is no difference on whole digital system between iKAGRA and bKAGRA. Timing of each RT PC for subsystem depends on the installation schedule of each subsystem. We need more detailed schedule for all related subsystem.

2-6. Risk Management

Here is a list of risks of this subsystem.

Cyber security: Probability 1, Seriousness 2

- We ask a professional level network security system to some companies.

Trouble shooting for huge number of channels: Probability 2, Seriousness 2

- We will design an enough redundant system and develop a self-diagnostic system.

Installation for subsystem: Probability 3, Seriousness 2

Not enough test of each subsystem outside the mine introduces some serious delay in the mine.

- We preapare for a simulate plant system for virtual control test before the installtion. We ask more detailed installation schedule for each subsystem, and we will provide enough prototype RT PCs.

Software bug: Probability 1, Seriousness 1

- LIGO has enough experience until eLIGO, and aLIGO people are frequently checking RT software with actual subsystems. We keep updating software.

Upgrade hardware: Probability 3, Seriousness 2

No budget for upgrading PC etc.

- We prepare some spare PCs. We ask another budget for maintenance. Maintenance for PCs may be done with data analysis group.

Since KAGRA decided to use aLIGO type digital system, we were relieved a lot of works, for example, selection of ADC/DAC modules, development of real time code, a loop test for control using combined RT control computers, I/O chassis and circuits. First of all, we thank LIGO CDS group for offering us such a useful device.

On the other hand, if we do not understand carefully inside of this device, everything can easily be a black box and very complicated and difficult system to hunt troubles for the future KAGRA construction. Fortunately we have been developed a prototype digital system for CLIO in these 2-3years with LIOG CDS group's corporations and we have experienced many things by constructing several RT PCs from the scratch. These experiences will be a great help for ourselves during the KAGRA commissioning.

Currently we are thinking that we have no serious problem to develop whole digital system for KAGRA. This digital subsystem is related to almost of all subsystems, and once a trouble happened on this system it can be a serious delay for the whole KAGRA. We continuously perform reliable operation tests and preparations for the smooth installation and the commissioning for KAGRA.

3. Design for bKAGRA

Essentially there is no difference for design of digital subsystem between iLIGO and bLIGO except for channel numbers. At the beginning of iKAGRA, the number of channels is very limited, and it will be increased during the development and commissioning of iKAGRA and bKAGRA.

3-1. Requirements

See section 2-1 on iKAGRA.

3-2. Preliminary Design

See section 2-2 on iKAGRA.

3-3. Schedule

See section 2-3 on iKAGRA.
The whole schedule including for iKAGRA and bKAGRA is shown in section 1-5 on bKAGRA schedule.

3-4. Prototype test

See section 2-4 on iKAGRA.

3-5. Quality assurance

See section 2-4 on iKAGRA.

3-6. Installation scenario

Essentially all digital subsystem components will be installed when iKAGRA starts. Installation procedure is explained in section 2-5 on iKAGRA.

3-7. Risk Management

See section 2-6 on iKAGRA.

Appendix A. Design changes that have been made with the suggestions in the 1st external review (if any)

It was pointed out in the last external review:

> The committee has some concern regarding the installation location adjacent to the interferometer vacuum chambers. Such proximity has led both the LIGO and VIRGO projects to relocate their electronics racks to separate rooms. We suggest considering the installation of all electronics in a separate rooms, as recommended in our discussion of the tunnel design.

We are developing a remote and fan less IO chassis connected by a fiber cable. The noisiest RT PCs can be located in separately isolated rooms and only IO chassis will located near the subsystem.

Appendix B. Items that have been reduced in cost (if any)

Not Applicable.

Appendix C. Human resources

C-1. Required man power (only for development, we need application users to develop subsystem models)

FY2012, 2013

- Computer hardware expert including network development: 2
- Computer software expert: 2
- Electronics: 2
- Simulated Plant (suitable for students): 1

FY2014, 2015

- Computer hardware expert including network development: 2
- Computer software expert: 2
- Electronics: 2
- Installation: 4

FY2016, 2017

- Computer hardware expert including network development: 2
- Computer software expert: 2
- Electronics: 2
- Upgrade: 4

FY2018

- Computer hardware expert including network development: 2
- Computer software expert: 2

Appendix D. Requirements

We estimate the requirement of dynamic range by a typical lock acquisition case and a typical error signal during observation.

1) During lock acquisition, the arm cavity moves ~1um. Finesse of the arm cavity is designed as ~1500, so the full width half maximum (FWHM) is ~1e-9m. When the cavity is locked the motion of cavity should be ~1/1000 of FWHM, so the motion will be roughly 1e-12m. Dynamic range should be > 1e-6m/1e-12m=120dB.

2) Amplitude of error signal during observation can be estimated by an expected seismic motion and a suppression factor by an expected control gain. Typically maximum seismic motion is expected as ~1e-5m/rHz and this low frequency motion is suppressed by a huge control loop gain. The suppression factor can be estimated by an expected unity gain frequency (UGF) = 200Hz and the gain slope of f^-4 between 1Hz and 100Hz, so the suppression factor can be easily obtained as 1e8. On the other hand, target sensitivity expected displacement noise will be 1e-21m/rHz, so the raw dynamic range will be 1e-5m/1e-21m = 1e16 = 320dB, and required dynamic range with the suppression will be 1e16/1e8 = 1e8 = 160dB. Additionally we can use whitening filters which typically consists of 2nd or 4th order of 15Hz-150Hz zero-pole filter, so effectively the whitening filter reduces the required dynamic range by 80dB with 2^{nd} order filter at least. So the assumption of 120dB dynamic range is enough. Note that the power line at 60Hz practically can be a big peak and may limit this dynamic range.