KAGRA

KAGRA 2nd External review for digital system subgroup

2012/4/19(Thu)

@ICRR 6F Large conference room

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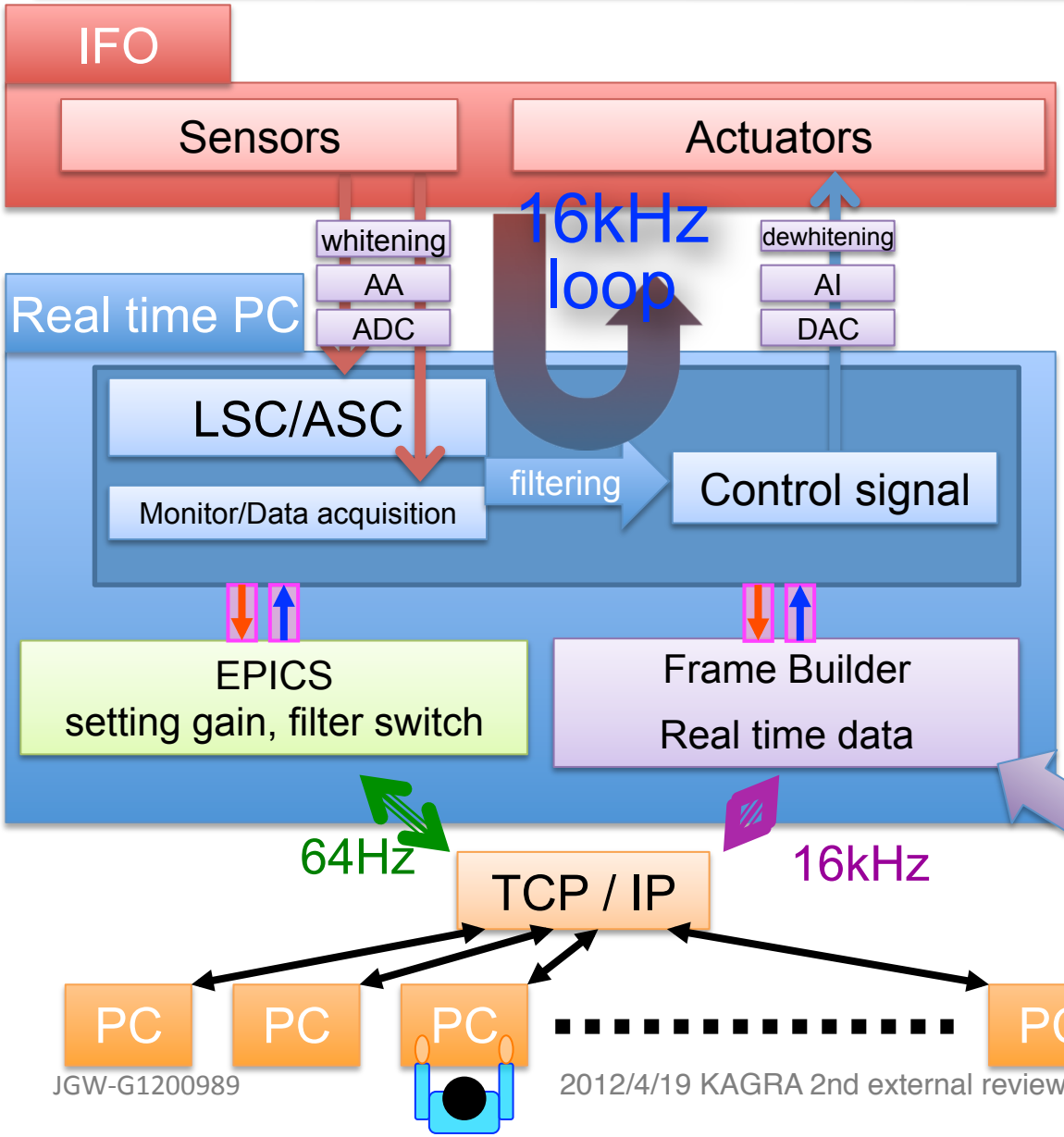
Yoichi Aso, Kiwamu Izumi, Masahiro Kamiizumi

Yuta Michimura, Shinji Miyoki, Naoko Ohishi

Naohiro Yamamoto, Hirotaka Yuzurihara

Overview: Concept of digital system



- Provides a very flexible human interface to the complex DOFs of the interferometer.
- Functions as sensing, control, monitor, switch
- Good solution to treat huge numbers of signals

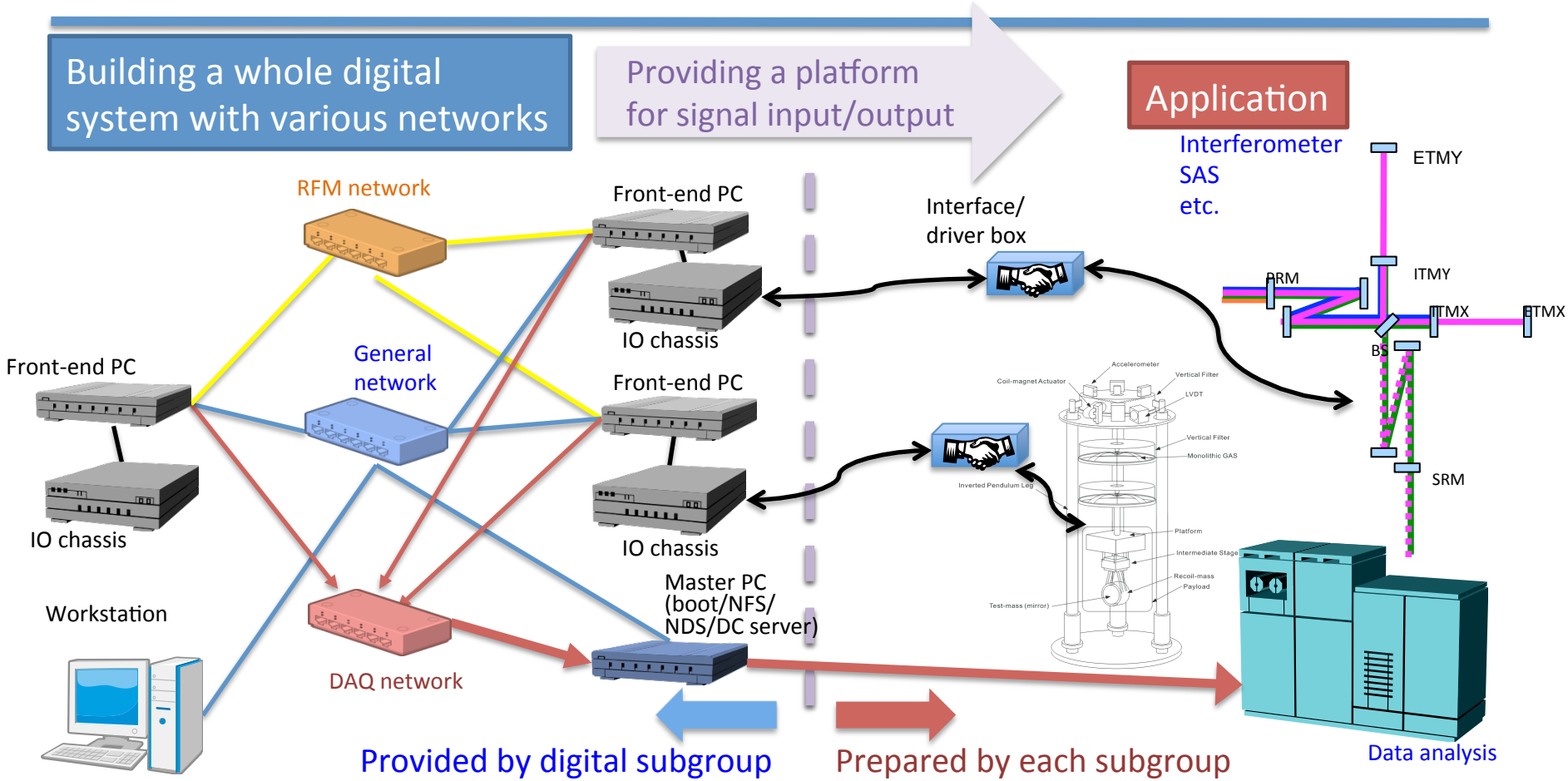
1-1. Definition and scope of the subsystem

Definition from SEMP(JGW-M1100465):

In charge of development of digital system to provide a flexible human interface for a km scale interferometer to all subsystems for controls, monitors, switches and diagnoses.

1. Function as Real time control
   - For complicated multiple DOFs
2. Function as Data acquisition system for GW waves
   - Control signal = GW data
3. Function as IFO tuning system
   - Reducing time for improving sensitivity
4. Function as Automatic IFO operation
   - Stable observation
5. Function as information collecting system for IFO
   - Automatic channel assignment for huge number of channels

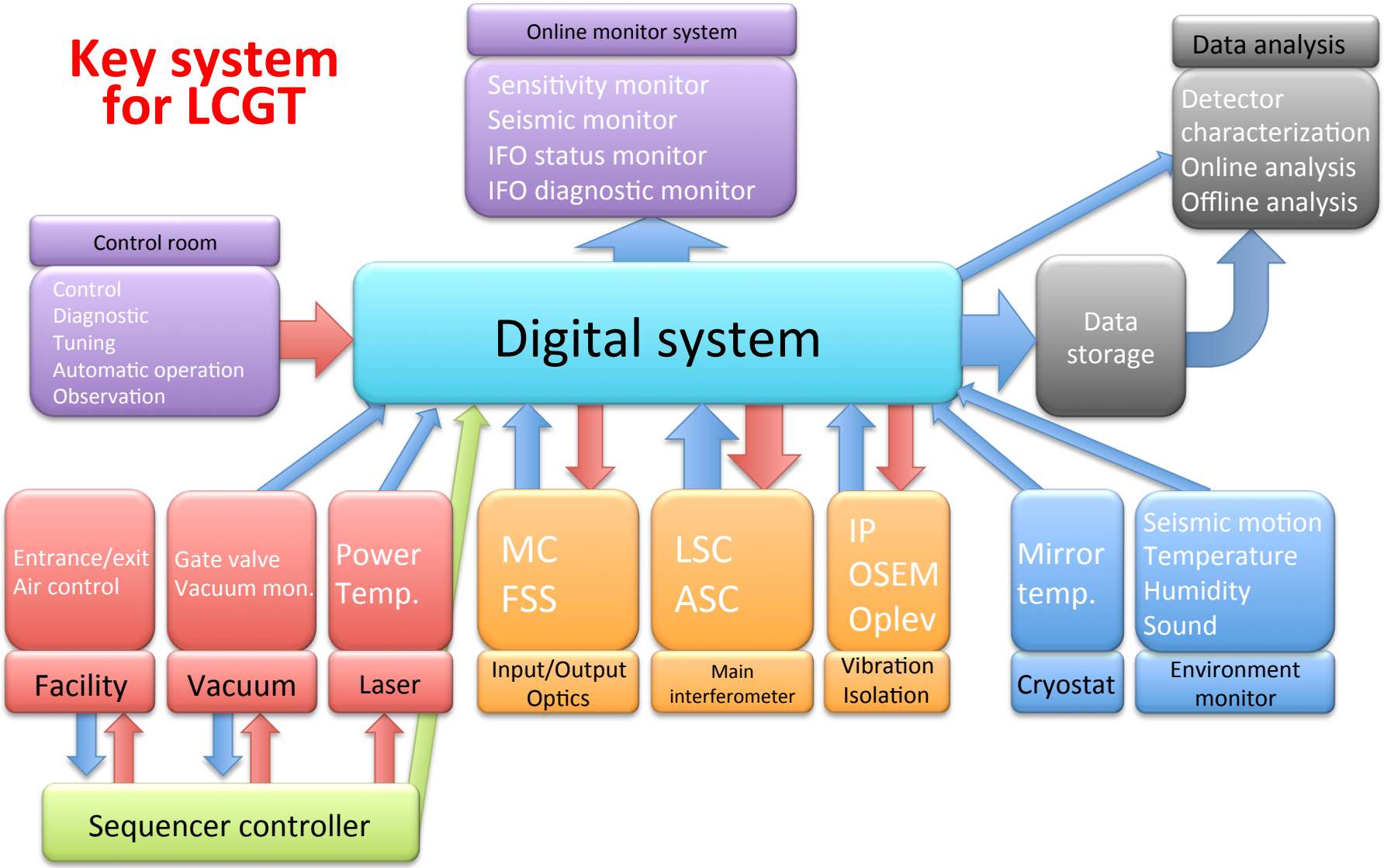
1-1. Definition and scope of the subsystem (cont'd)



- Real time system
- PC, software
- ADC/DAC/BO, AA/AI
- DAQ/RFM/timing network

- Control, monitor, switch
- Auto lock, auto alignment
- Commissioning, noise hunting
- Diagnosis, tuning, calibration
- Operation, observation

1-2. Important interface



1-3. Design phase: Pending items

Not many

- Slow EPICS controller
- Simulated plant

2-1. Target specification

Global requirements

- Observation bandwidth >5kHz
- Dynamic range >120dB
- Control bandwidth >200Hz
- Number of channels >1024
- Number of output channels >256

Internal requirements

Item	Requirements	Comment
Sampling rate	>=16384Hz	65536Hz at ADC, then decimated to 16384Hz
ADC bit resolution	>=16bit	
Dynamic range of input	>=+/-15V	Differential input
Dynamic range of output	>=+/-10V	Differential output
ADC noise	<3uV/rHz	Effectively reduced by whitening filter
DAC noise	<3uV/rHz	Effectively reduced by dewhitening filter
time delay	<100usec	For >200Hz UGF
Input channel numbers	>2048ch	(16kHz:>128ch, 2kzHz:>512ch, 64Hz>1024ch)
Output channel numbers	>512ch	For mirrors, seismic attenuators, PZTs etc.
Stored channel numbers	16kHz:>64ch, 2kzHz:>512ch, 64Hz>1024ch, 16Hz>10000ch	~300TB/year

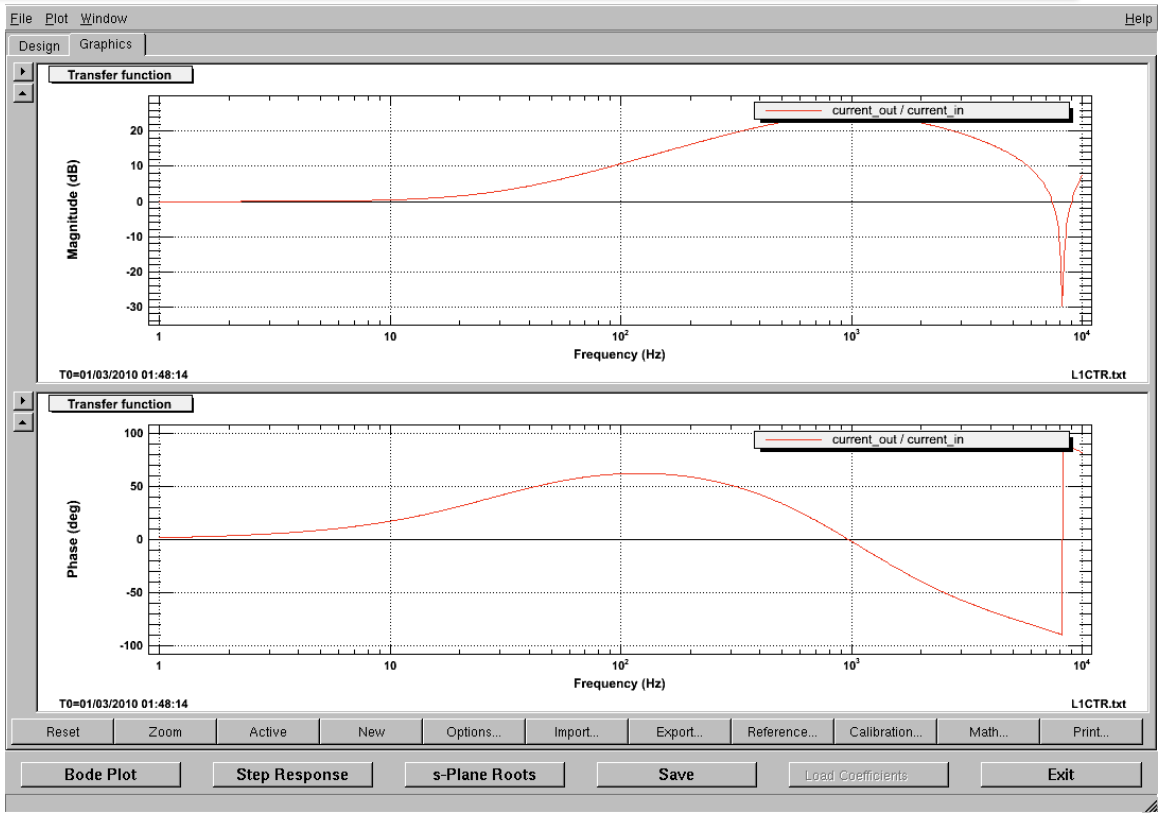
Provides a robust and flexible platform to IFO and all subsystems for control, monitor, diagnostic, switch during installation, commissioning, operation, observation

2-1. Target specification: hardware

1. Dual x86 processors, with four CPU cores each.
2. Processor clock speed of ~3GHz.
3. Minimum 8 Gigabyte of memory.
4. Two Gigabit Ethernet interfaces.
   - General TCP/IP
   - DAQ network by Myrinet or Open-MX protocol
5. One, or more, real-time network interfaces
   - Reflected Memory (RFM)
   - PCI Express (PCIe) network interface
6. A PCIe interface to the PCIe expansion chassis with a maximum of 10 PCIe cards installed.

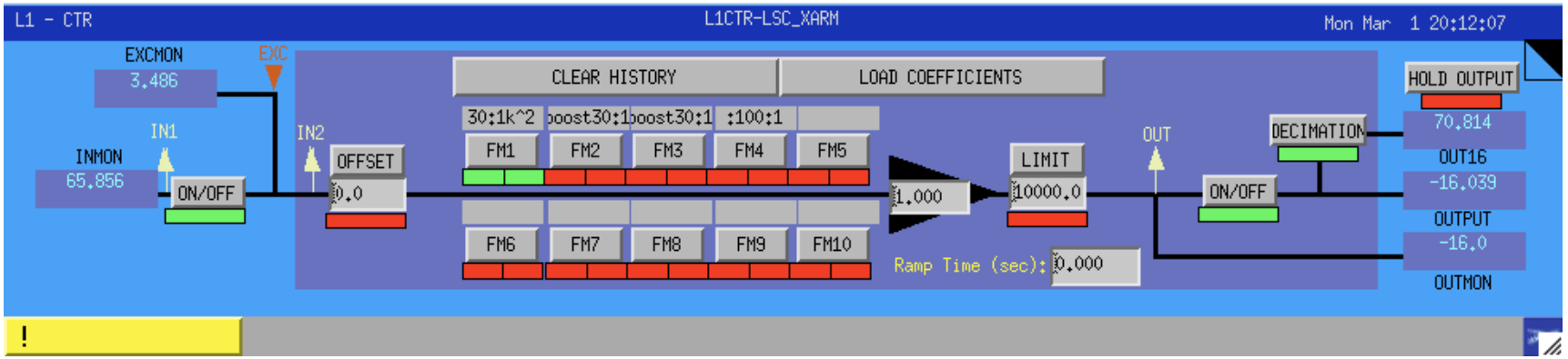
2-1. Target specification: software

- Dataviewer: osciloscope,
- DTT: FFT analyzer
- Foton: digital filter composer
- Ezcademod: digital modulator/ demodulator
- Foton: GUI digital filter composer

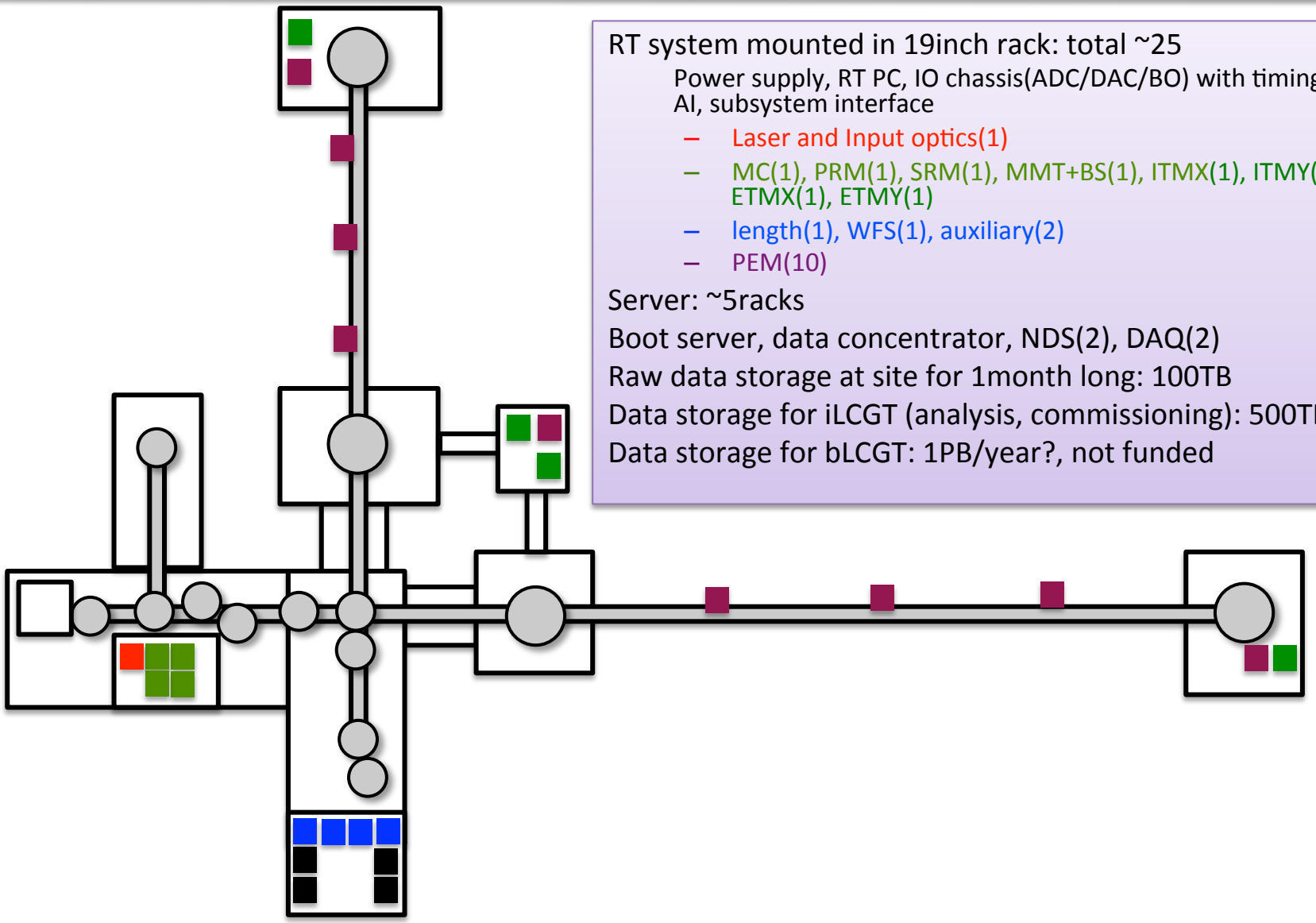


Filters on MEDM

- Signal excitation
- 10 filter banks
- 3 monitor point IN1/IN2/OUT



2-2. Final design: RT rack position



RT system mounted in 19inch rack: total ~25

Power supply, RT PC, IO chassis(ADC/DAC/BO) with timing, AA/AI, subsystem interface

- Laser and Input optics(1)
- MC(1), PRM(1), SRM(1), MMT+BS(1), ITMX(1), ITMY(1), ETMX(1), ETMY(1)
- length(1), WFS(1), auxiliary(2)
- PEM(10)

Server: ~5racks

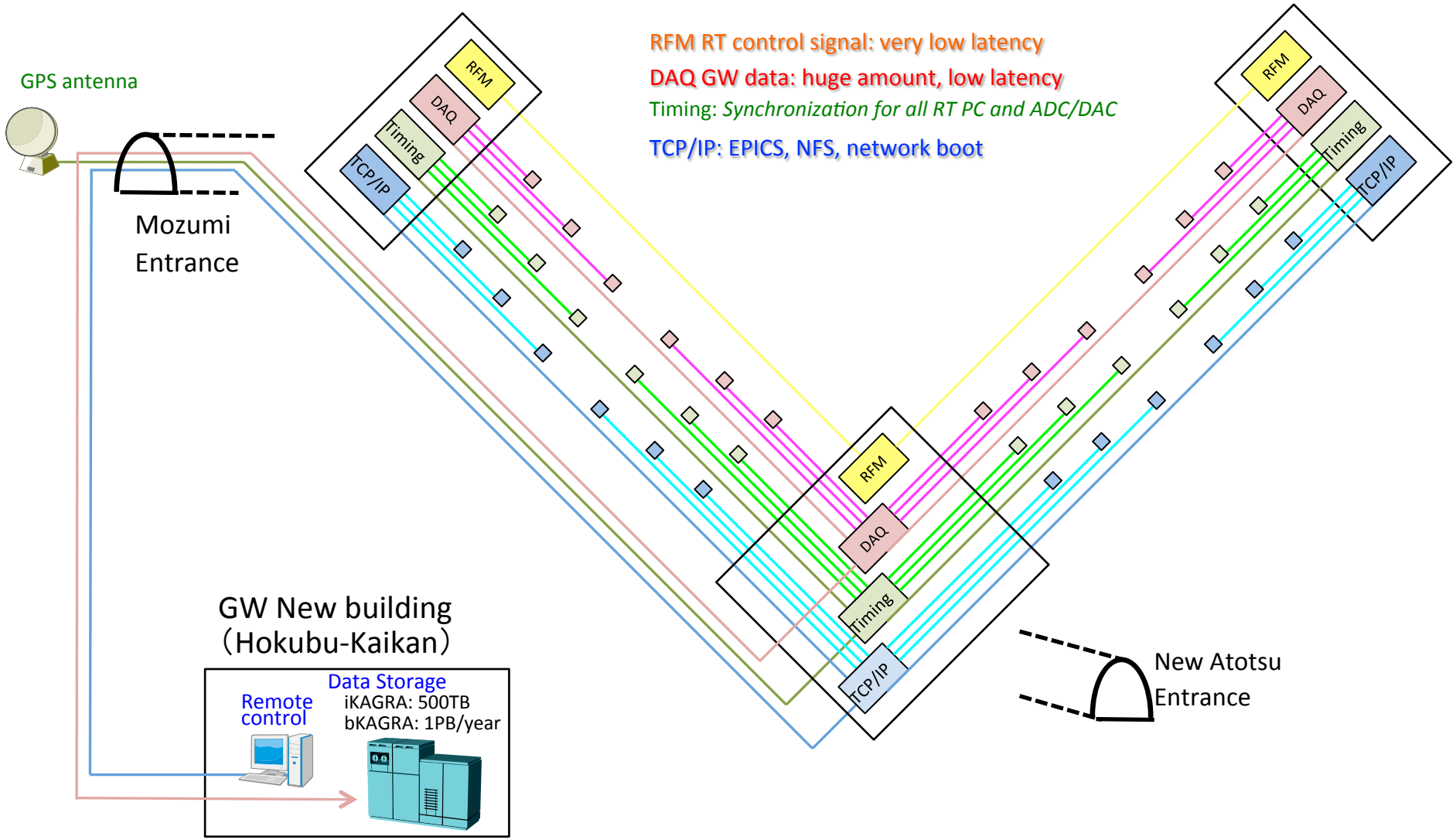
Boot server, data concentrator, NDS(2), DAQ(2)

Raw data storage at site for 1month long: 100TB

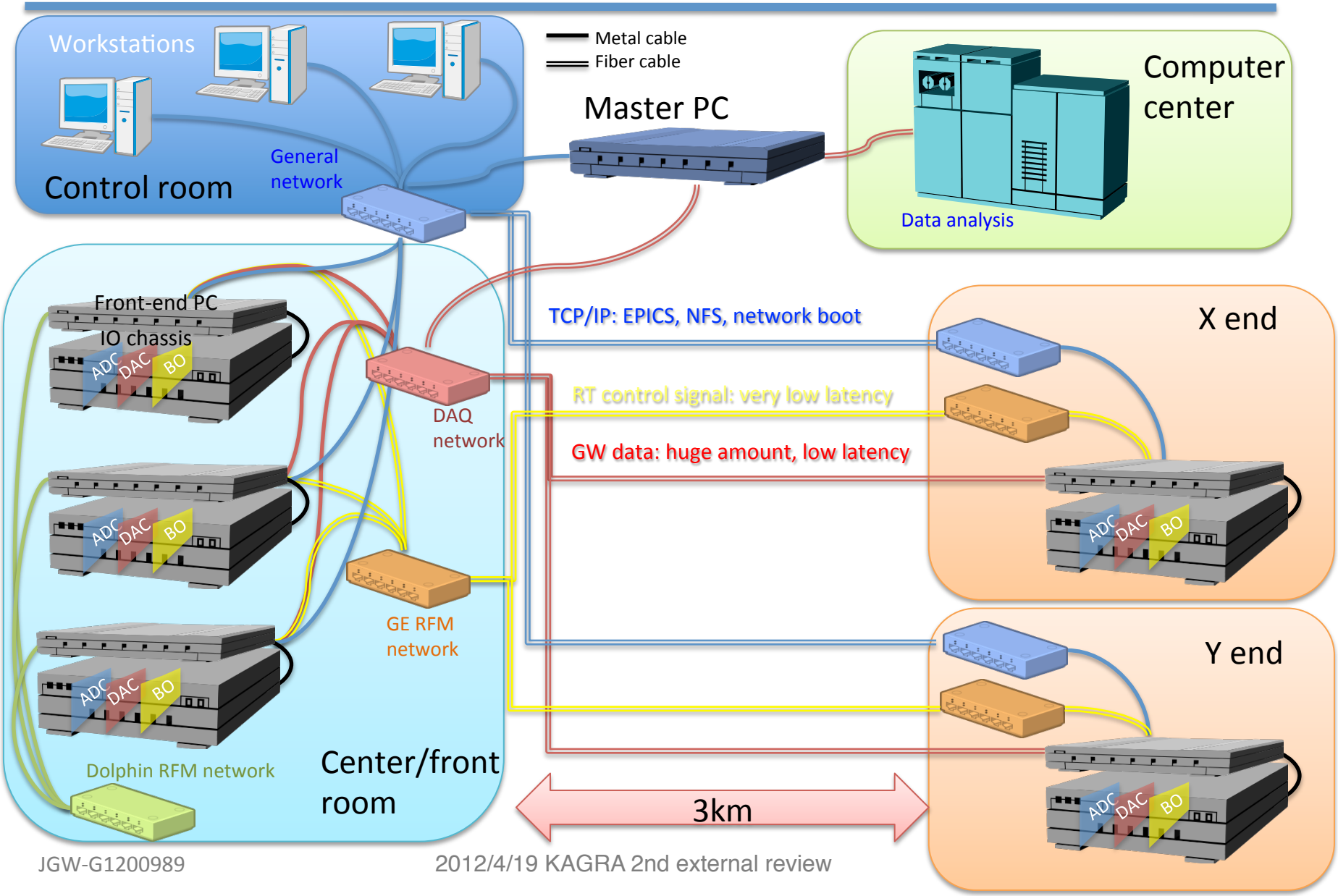
Data storage for iLCGT (analysis, commissioning): 500TB

Data storage for bLCGT: 1PB/year?, not funded

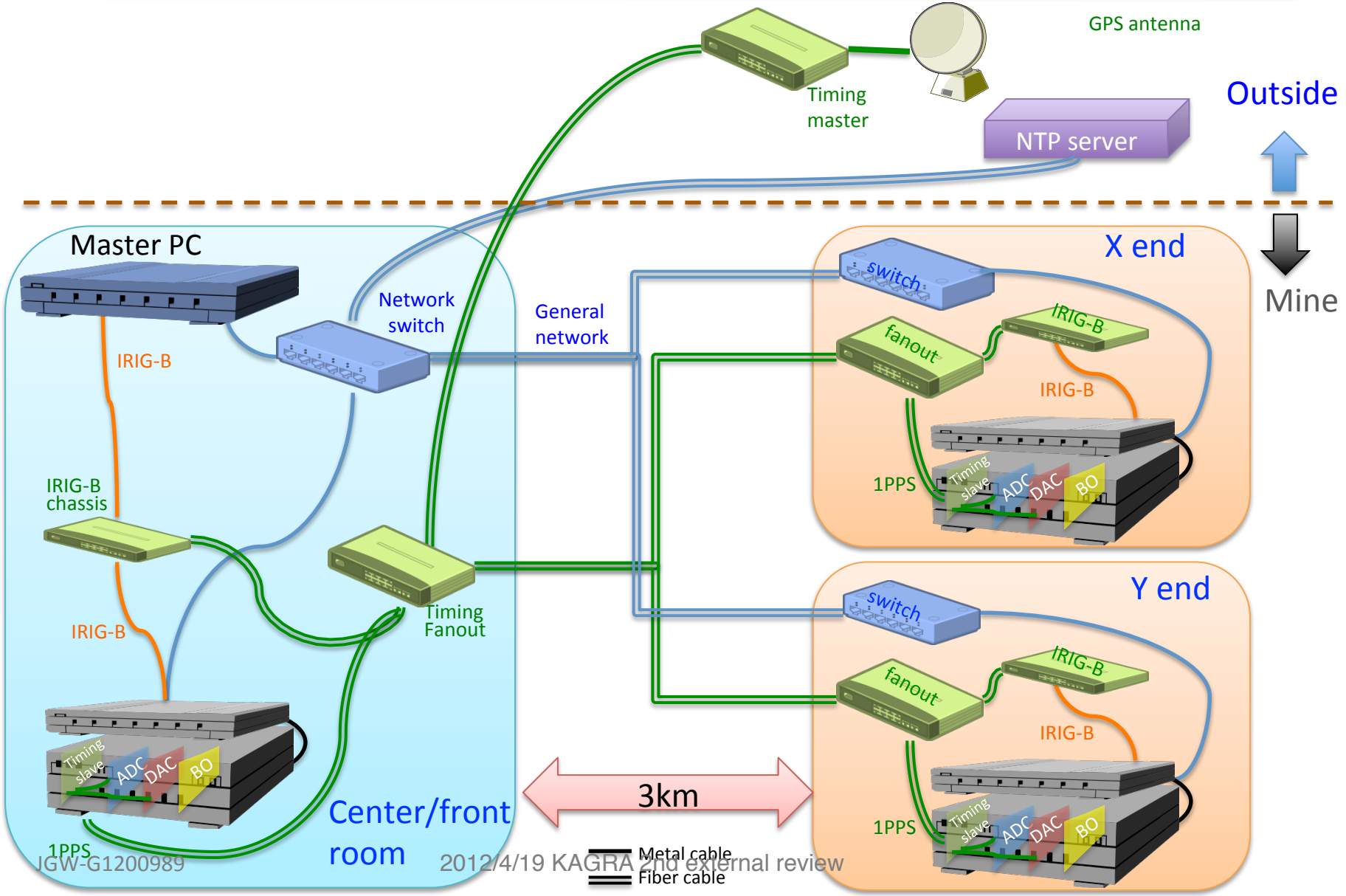
Network design



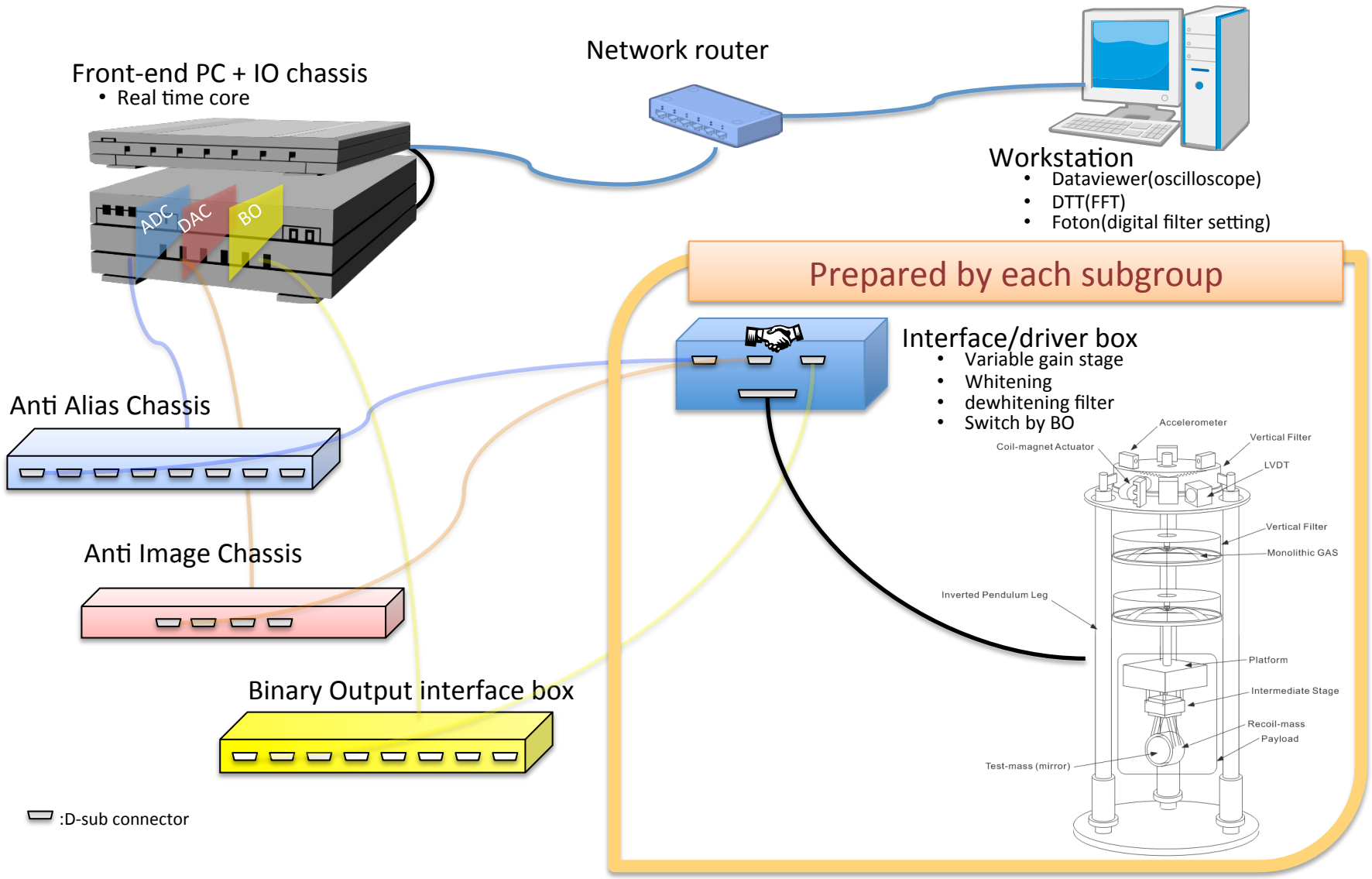
2-2. Final design: Network design



2-2. Final design: Timing Network



2-2. Final design: Connecting to subsystems



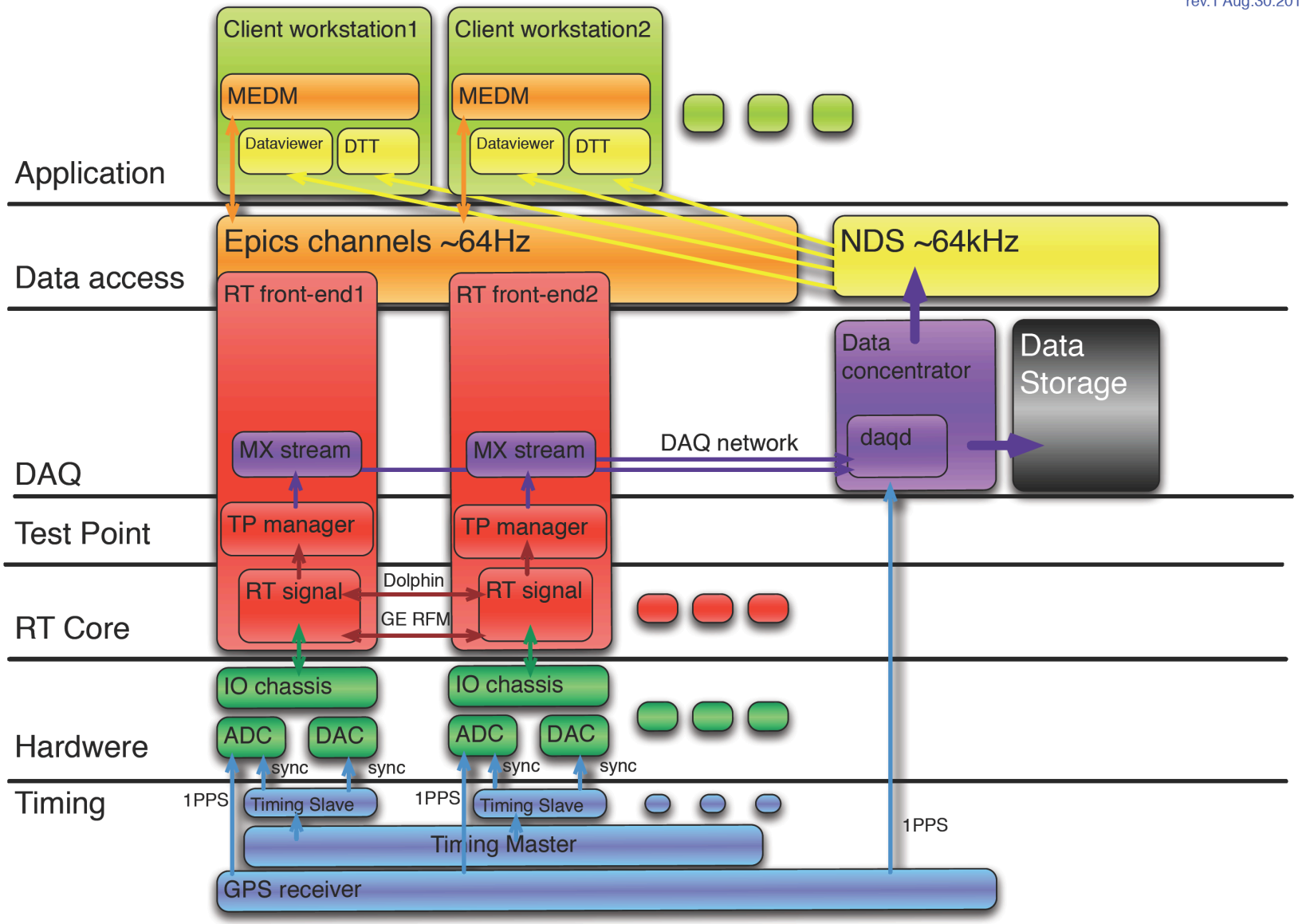
2-2. Final design: Interface

- ADC 32ch/card
  - 16kHz sampling
  - With Anti Alias filters
  - 2uV/rHz
  - D-sub 9pin(for 4ch, differential), +/-20V input
- DAC 16ch/card
  - With Anti Imaging filers
  - 1.5uV/rHz
  - D-sub 9pin(for 4ch, differential), +/-10V output
- BO 32ch/card
  - D-sub 9pin(for 4ch, differential), 0 or +5V output
    - Ex. Variable gain amp for 16 steps/1 D-sub connector
- Pico/stepping motor controller using slow EPICS

Note: D-sub 37pin may be supported for all input/output

LCGT Digital System Layer Map

JGW-D1100588
rev.1 Aug.30.2011



JGW-G1200989

Slow EPICS system for Physical Environmental Monitors

- Agreed to use RT system as PEM DAQ
  - Current RT system can be used since fiber cables exist every 500m in the arm
- Needs pico motor controller
  - tested at CLIO, but using single PC
- Multiple PCs for Pico/stepping motor and PEM
  - Another PCs at each vacuum chamber?

Making channel lists

- Needs channel list for ADC/DAC/BO
  - ADC input ~2048ch
    - will be categorized as class1(IFO main), class2(IFO sub), class3(PEM, physical environment monitor)…
  - DAC output: ~512ch
  - BO: ~2048ch
- DAQ channel: stored signals to data storage as 16kHz, 2kHz, 64Hz…

DAQ Channel list

	Number of stored channels	Data acquisition, Data analysis, IFO control	16kHz:64ch, 2kHz:512ch, 64Hz:1024ch 16Hz:16384 epics channels (see channel list)
*	Data bit resolution at ADC/DAC	Data acquisition	16bit = 65536
*	Data bit resolution in PC	Data acquisition	32bit = 4 Byte integer
	Data transfer rate	Data acquisition	4MB/sec for 16kHz, 4MB/sec for 2kHz, 128kB/sec for 64Hz, 1MB/sec for 16Hz, Total ~10MB/sec ~30GB/hour ~1TB/day ~300TB/year

6. Channel list

a. 16kHz (total 64ch)

Part	Channel point	Channel number	Description
Laser	Output laser power[W]	1	
	IFO Input laser power[W]	1	
MC	REFL	1	
	MC length feedback	1	
	MC frequency feedback	1	
LSC	I&Q dor DARM, CARM, MICH, PRC, SRC, etc.	10	
	error, feedback	10	
SUS	length * 10 suspensions	10	

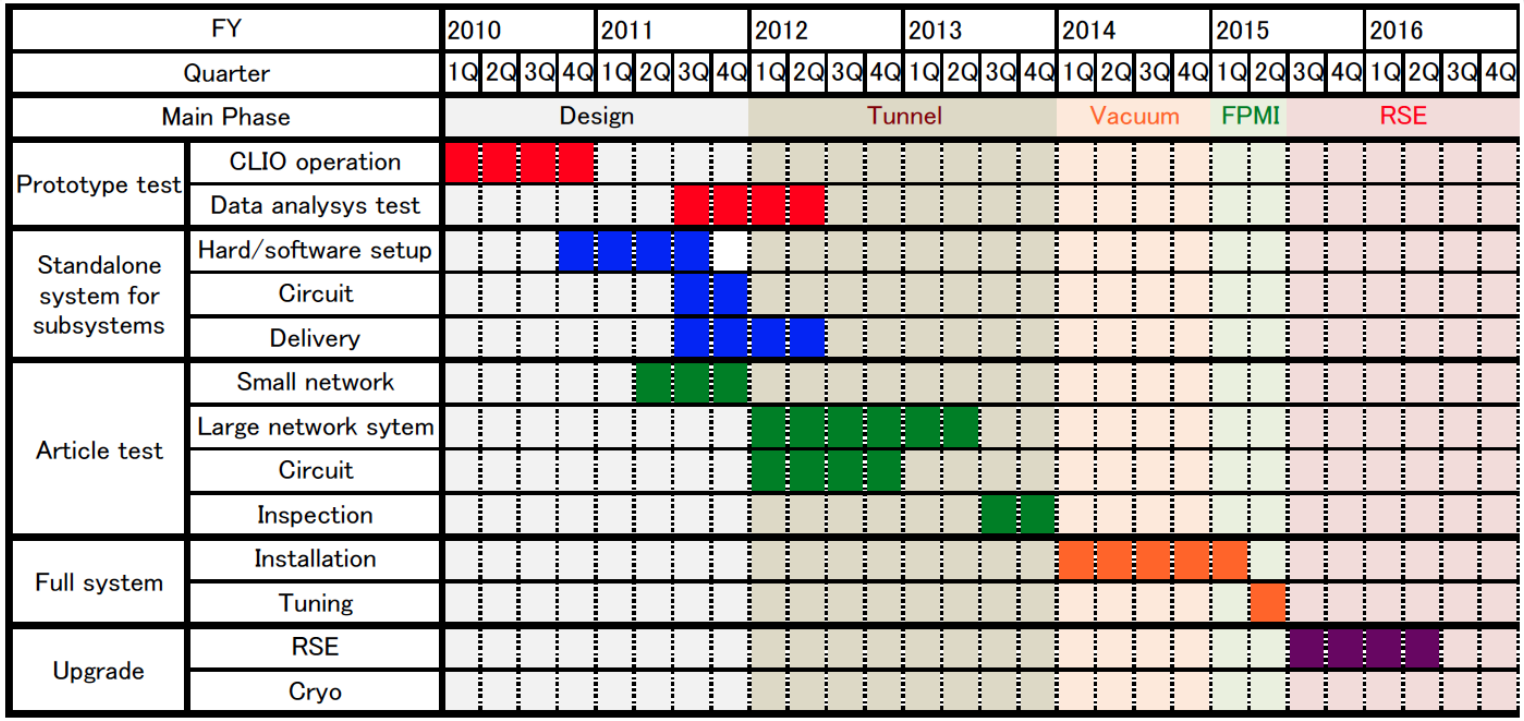
b. 2kHz (total 256ch)

Part	Channel point	Channel number	Description
ASC	WFS	5xpitch, yaw=50	
	Oplev	10xpitch,yaw=100	

c. 64Hz Long term monitor (total 512ch)

Part	Channel point	Channel number	Description
Temperature[deg]	room	10	center, end, arm
	table	10	laser, REFL, AS, pickoff, end
	suspensions	50	Low temperature
	mirrors	50	Low temperature
Humidity[%]	rooms	10	center, end, arm
Dust	rooms	10	center, end, arm
Laser	crystal temperature[degree] and etc.	10	
	Master laser power[W]	2	

2.3 Schedule for KAGRA RT control
2.4 Quality assurance



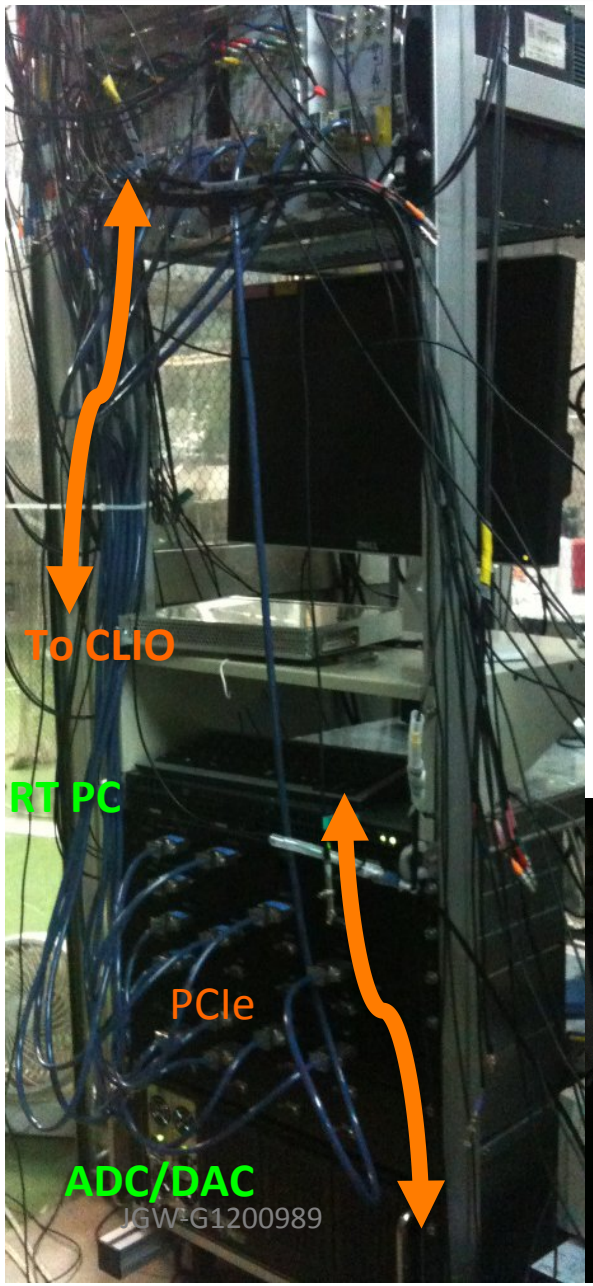
A. 2009-2010 prototype test @ CLIO (done)
   - Basic IFO operation and noise performance
B. 2011~ standalone system for subsystem (system: done, 2/5 delivered)
   - Data analysis, VIS, (IOO, CRY…)
C. 2011 Small network test with 1 master and 2 RT PCs (done)
   - GE RFM, Dolphin RFM, DAQ, timing network
D. 2012-2013 Full test@ Kamioka new building
   - Constructing many RT rack modules

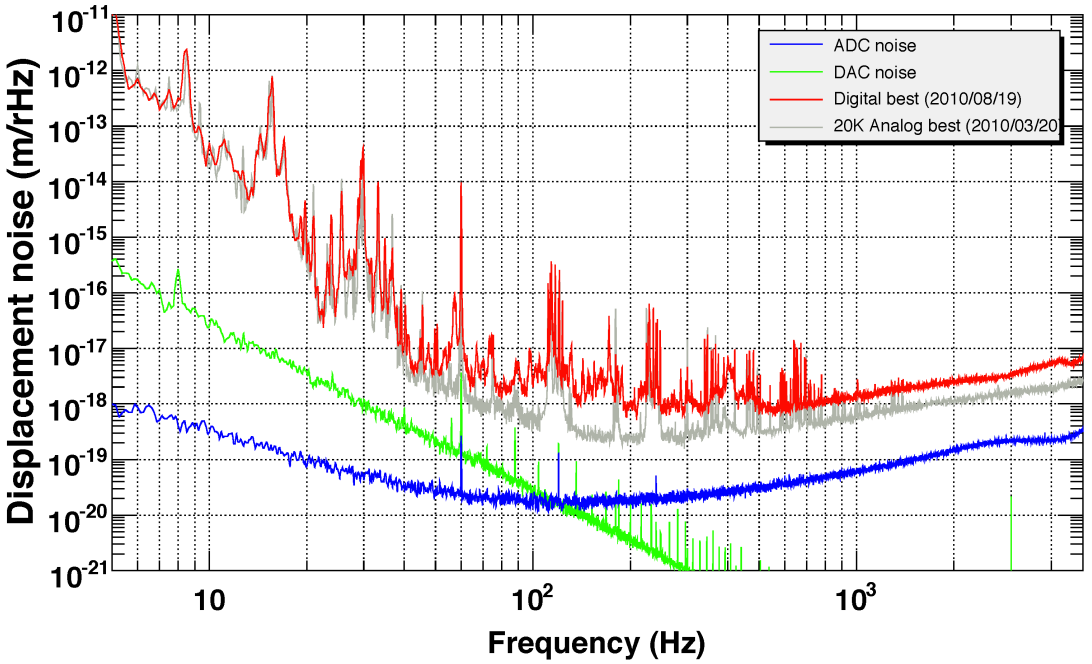
Installation into KAGRA mine

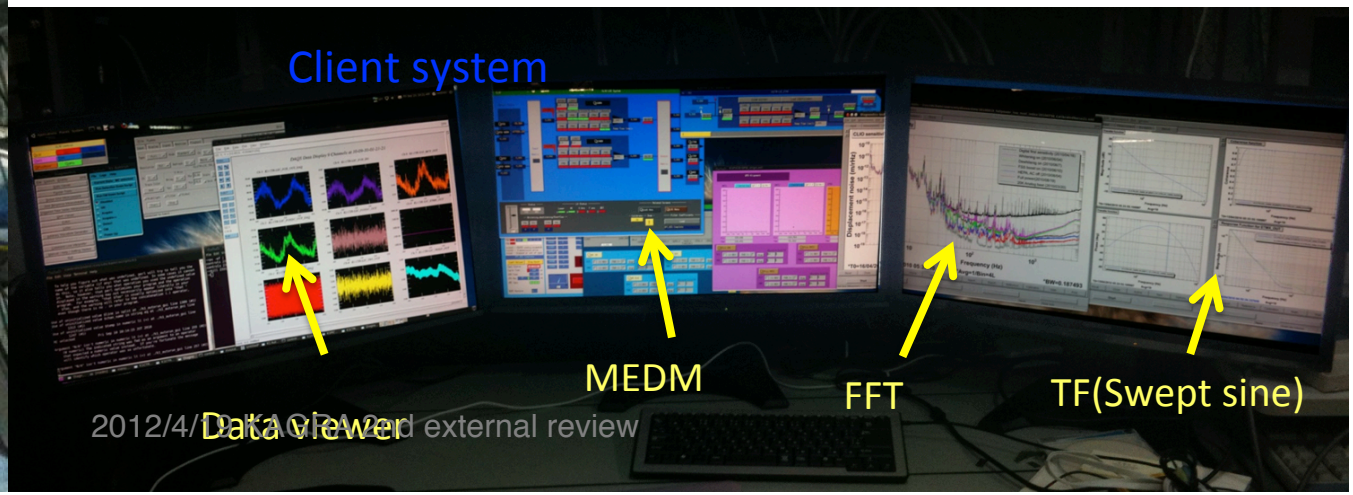
2.4 Quality assurance: A. Prototype test @ CLIO

- Setting up Real-time control computers
  - Obtaining equipment in Japan like ADC/DAC/BO, IO chassis…
- Related analog circuits like AA/AI, WF/DWF
- Lock acquisition
  - linearizing error signal
  - normalizing power
- Calibration process on DTT
  - sensitivity monitor
- Noise performance
  - Switching WF/DWF by BO
- Auto alignment using Python based Pico motor controllers on EPICS
- Application for other R&D experiment

2.4 Quality assurance: A. Prototype test @ CLIO







2.4 Quality assurance:
B. Standalone system for subsystems

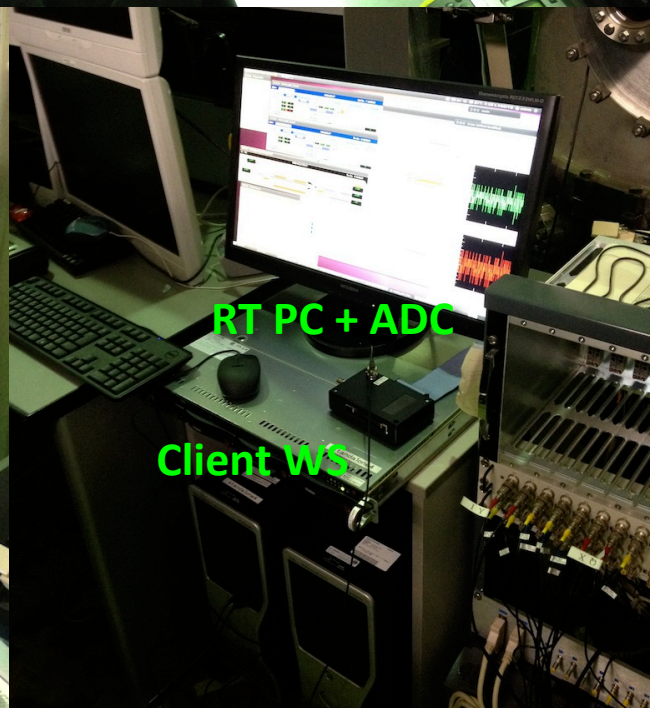
5sets of stand alone digital system will be delivered to subgroups in FY2011-2012

1. Real time control computer as front-end
2. Client workstation PC with software setup
3. PCIe I/O chassis for ADC/DAC/BO modules
4. Timing slave board
5. ADC, DAC, Binary Output
6. Anti Alias/Anti imaging filters, BO interface

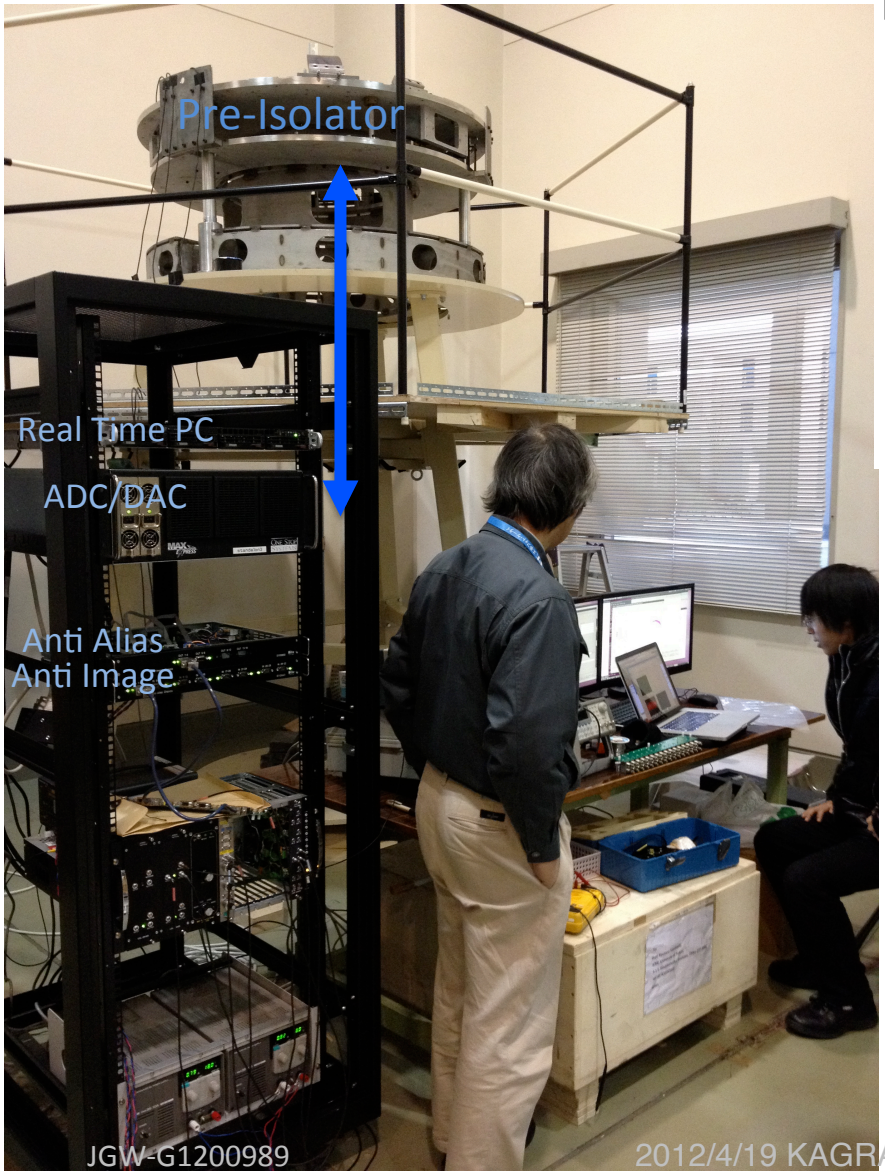
- good chance for subgroups to be accustomed with a digital system before the commissioning of LCGT

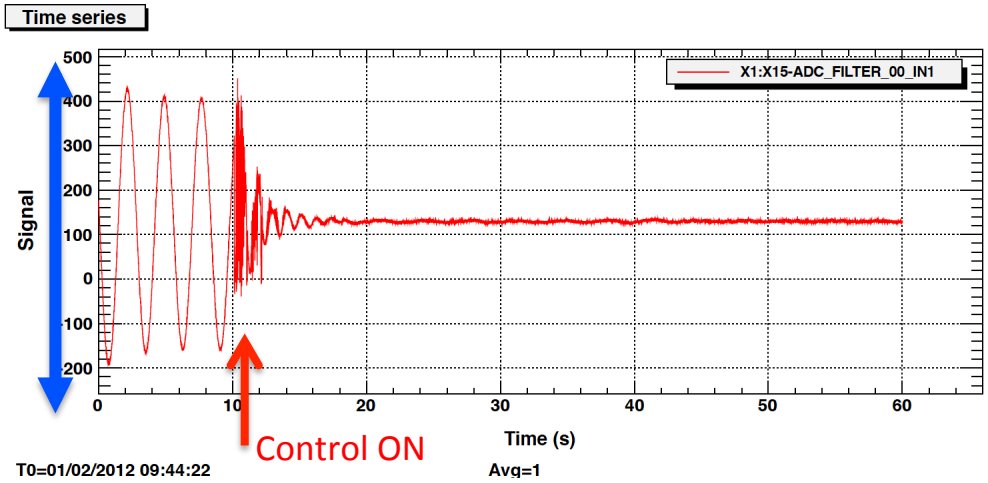
2.4 Quality assurance:
B. Standalone digital system for online data analysis

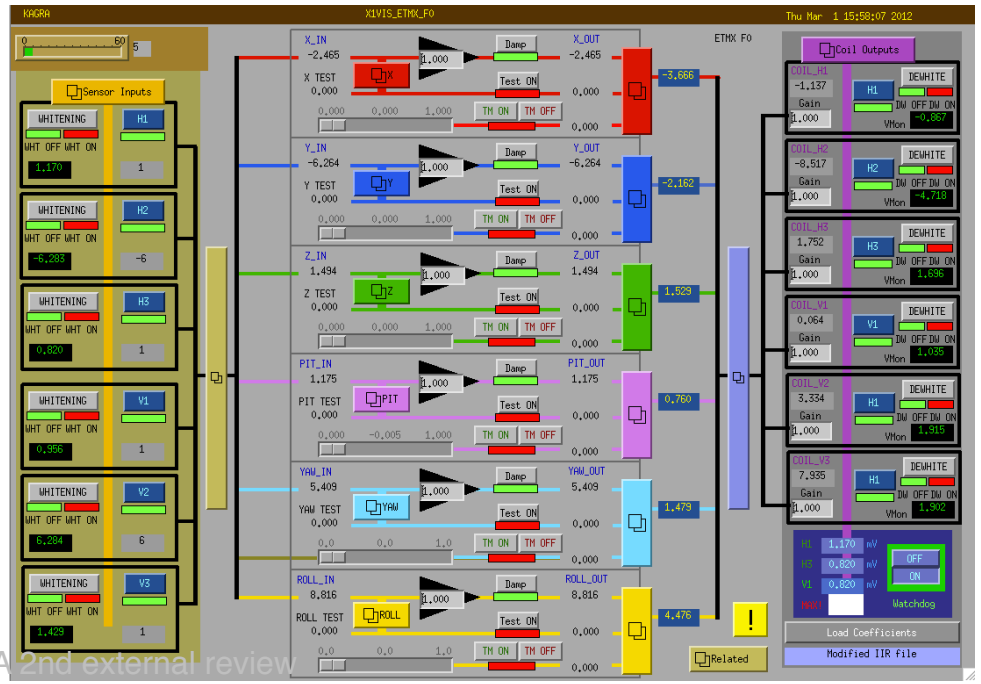
- Simple standalone system (RT PC + ADC, Client WS, router) has been delivered to NAOJ on 12/6/2011.
- 3days work for installation, lecture and training
- Online analysis software will be developed by DAS group.



2.4 Quality assurance:
B. Digital control system for Pre-Isolator







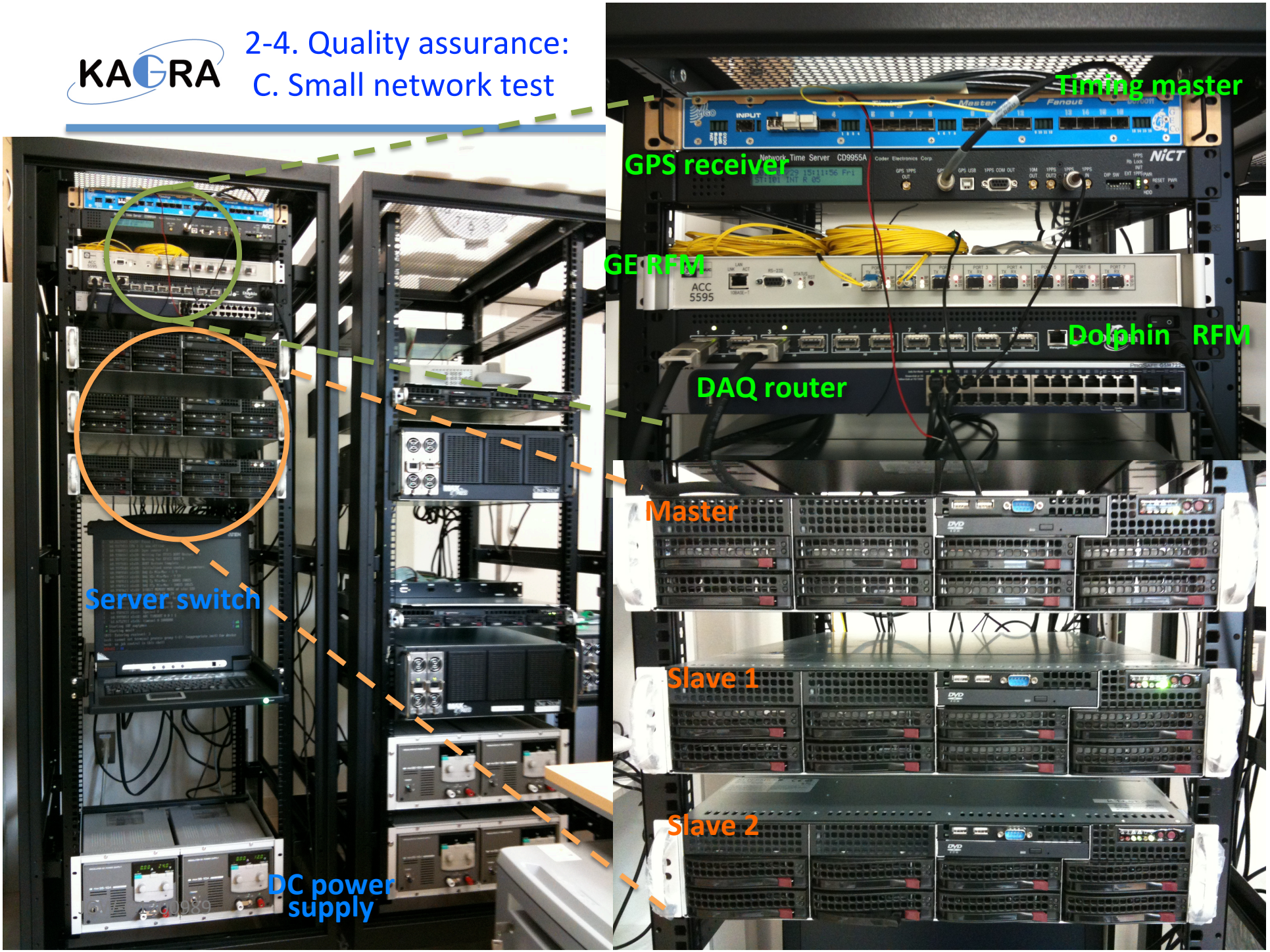
2.4 Quality assurance: Preparation for mass production of circuits for DGS

- 8 D-SUB 9pin connectors as 32ch signals input at front panel for AA (ADC)
- 4 D-SUB 9pin connectors as 16ch signals output at front panel for AI (DAC)

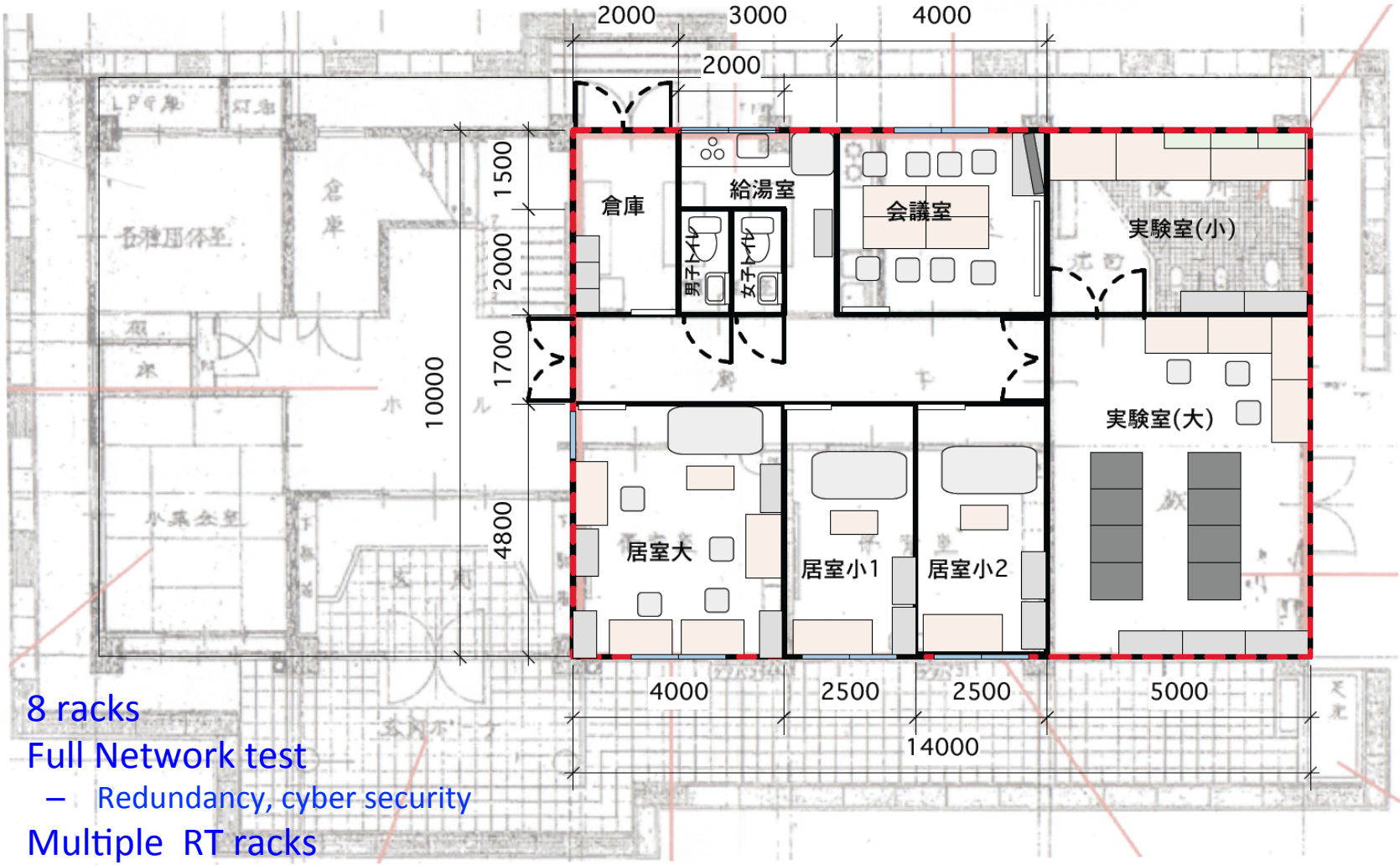
- SCSI 68pin connector as input/output at rear panel
- D-SUB 3pin connector as DC power supply input
- 0.2A/card

- AA and AI for VIS are ready.
- 6 AA and 6 AI will be made in this FY.

2-4. Quality assurance: C. Small network test



2-4. Quality assurance: D. Full test at Kamioka



- 8 racks
- Full Network test
  - Redundancy, cyber security
- Multiple RT racks

2-4. Quality assurance: Full system

All below items are being discussed and will be ordered as a full LCGT control system

- ADC ~100, DAC ~50, BO ~100
- AA ~100 chassis, AI ~50 chassis, BO interface ~50 chassis
- Remote IO chassis ~30
- RT PCs ~30
- Server PCs ~10
- Control WSs ~10
- Data storage (~500TB)
- Network switches
- Timing system
- Full channel test
- 3km test
- Security, redundancy

2-5. Installation scenario: Construction of full digital system

- Installation of whole system: just moving from Kamioka new facility into LCGT mine in the middle of FY2014
- Installation of RT racks for subsystem
  - Making a RT rack module:
    - RT PC, IO chassis, AAs, AIs, BO interfaces, power supply,
  - Add RT racks to full system (network boot)
  - When?
    - depends on the installation of subsystems.
- Commissioning
  - Cable
  - Wiring
  - Noise level, TF check
- Maintenances
  - Software update
  - Hardware upgrade (ex. LIGO: every 3 or 4 years)

2-6. Risk management

- Cyber security: P=1, S=2 -> R=2
  - Needs professional level network security system
- Huge number of channels: P=2, S=2 -> R=4
  - How do we check huge number of channels for analog and digital to avoid troubles?
  - Make fully redundant system
- Commissioning on site without tested by subgroup: P=2, S=2 -> R=4
  - Simulated plant
- Bug on RT core or other related software: P=1, S=1 -> R=1
  - Fully tested at iLIGO, eLIGO, and currently being tested at aLIGO subsystems
- Spare hardware for trouble and upgrading: P=3, S=2 -> R=6
  - Some spare PCs will be prepared, but no budget for upgrading

The estimated probability P:

0 The probability is extremely low and will almost never occur.
1 The probability is not large and will probably not occur.
2 The probability is around 0.5.
3 The probability is large and will probably occur.

The degree of seriousness S:

0 It will not affect the successful completion of the project.
1 It will to some degree affect the successful completion of the project.
2 It will to some degree endanger the successful completion of the project.
3 It will result in the failure of the project.

If the degree of risk R = P x S is equal to or larger than 2, show backup plan.

Needs more manpower

- Activity for development: Miyakawa (whole) and Kamiizumi (circuits)
- Activity as users: Hayama (data pipeline), Michimura (R&D), Takahashi (VIS)

  (Official members: Miyakawa, Aso, Izumi, Kamiizumi, Michimura, Miyoki, Ohishi, Yamamoto, Yuzurihara)

- Needs more developers in the next 2 years for important development term
  - Development for Slow EPICS controller
  - Circuits design for subsystem's interface including whitening/ dewhitening and variable gain amplifier
  - Simulated plant (for students?)
  - Computer hardware expert including network
  - Computer software expert
  - Commissioning people

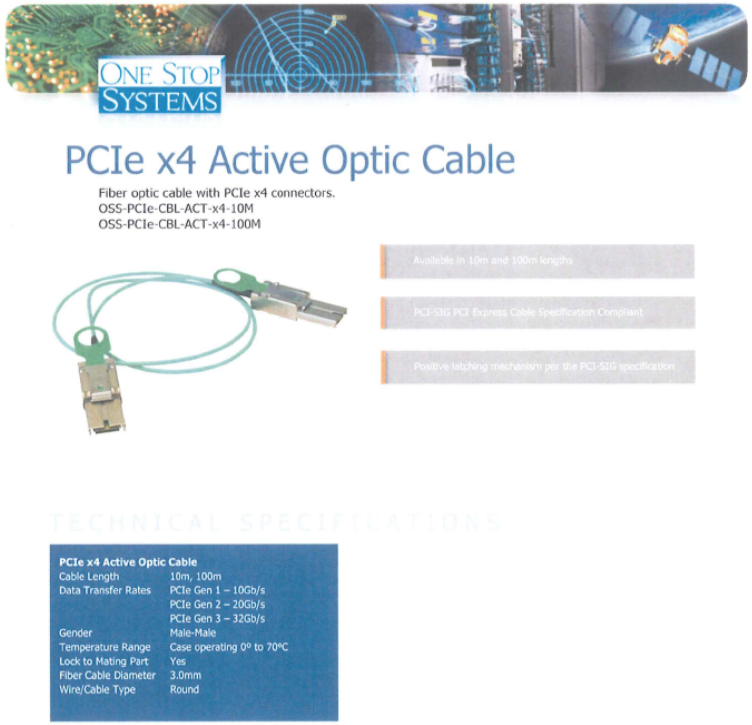
3. bLCGT

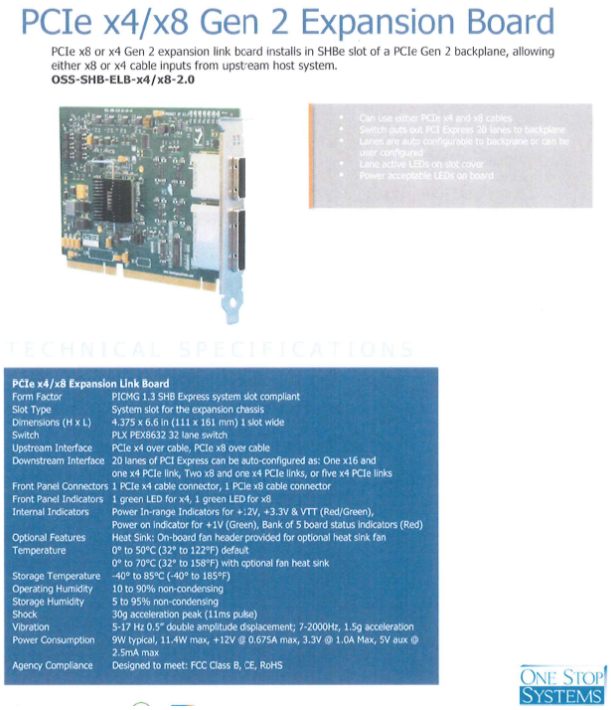
- Essentially no difference for digital subsystem between bLCGT and iLCGT because of budget limitation.
- We will install all RT computers, client WSs, network computers and networks(RFM, timing, DAQ, general) when iLCGT is installed.
- Channel number will be limited at the installation of iLCGT and it grows up during commissioning of iLCGT and bLCGT.
- Upgrade for hardware should be considered. Ex. LIGO is planning to replace PCs every 3-4 years. In any case, initial design can support bLCGT spec.

Appendix A. Design changes that have been made with the suggestions in the 1st external review

Development for Remote IO chassis

The committee has some concern regarding the installation location adjacent to the interferometer vacuum chambers. Such proximity has led both the LIGO and VIRGO projects to relocate their electronics racks to separate rooms. We suggest considering the installation of all electronics in a separate rooms, as recommended in our discussion of the tunnel design.





- No fan for calm environment
- Development and test with 6 prototypes in FY2011, FY2012
- IO chassis test for ADC/DAC and BO with existing aLIGO type timing system for short/long distance

Appendix B. Items that have been reduced in cost (if any)

None