



Internal review for digital system subgroup

2012/1/27(Fri)

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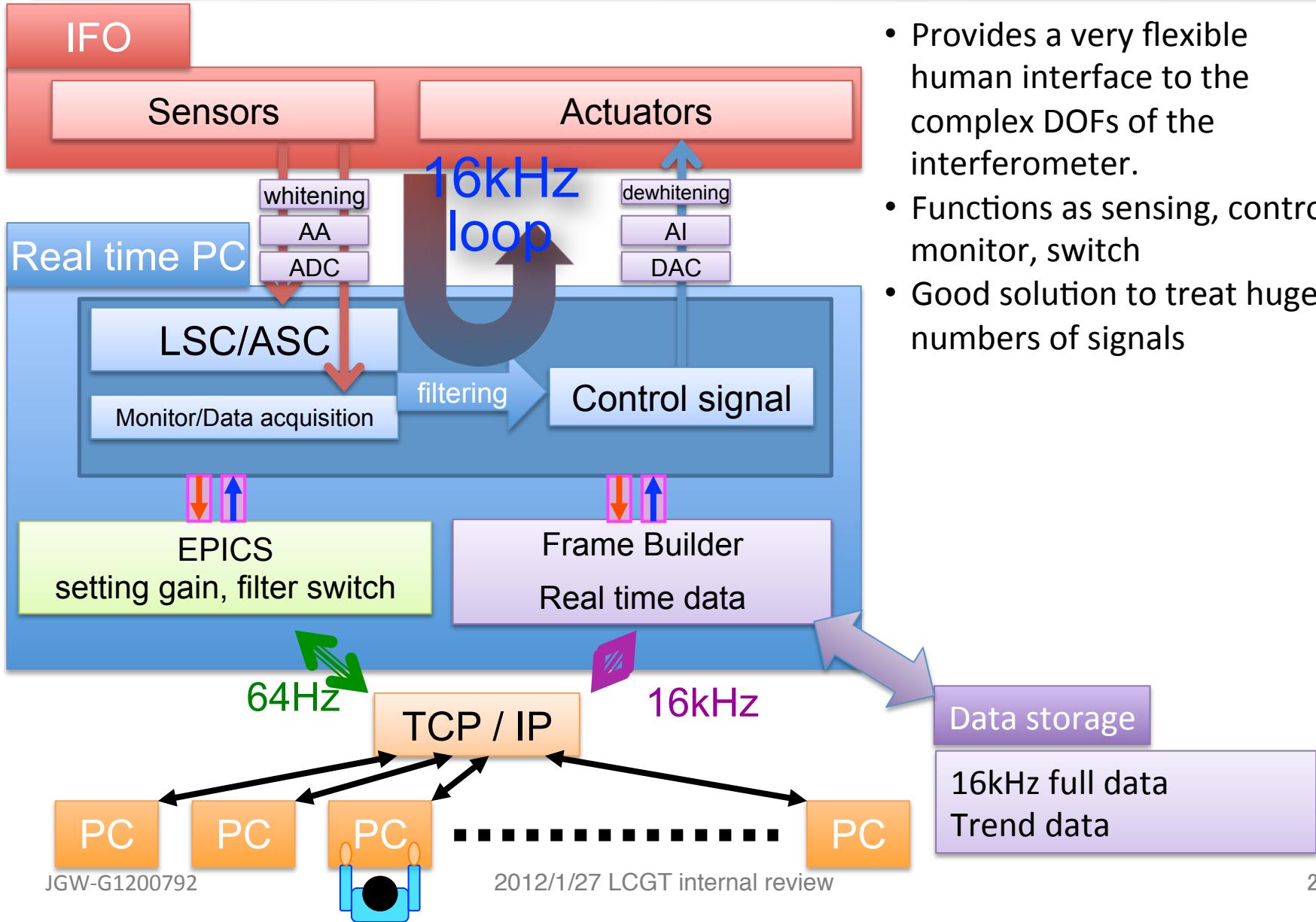
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Overview: Concept of the digital system





1-1. Definition and scope of the subsystem

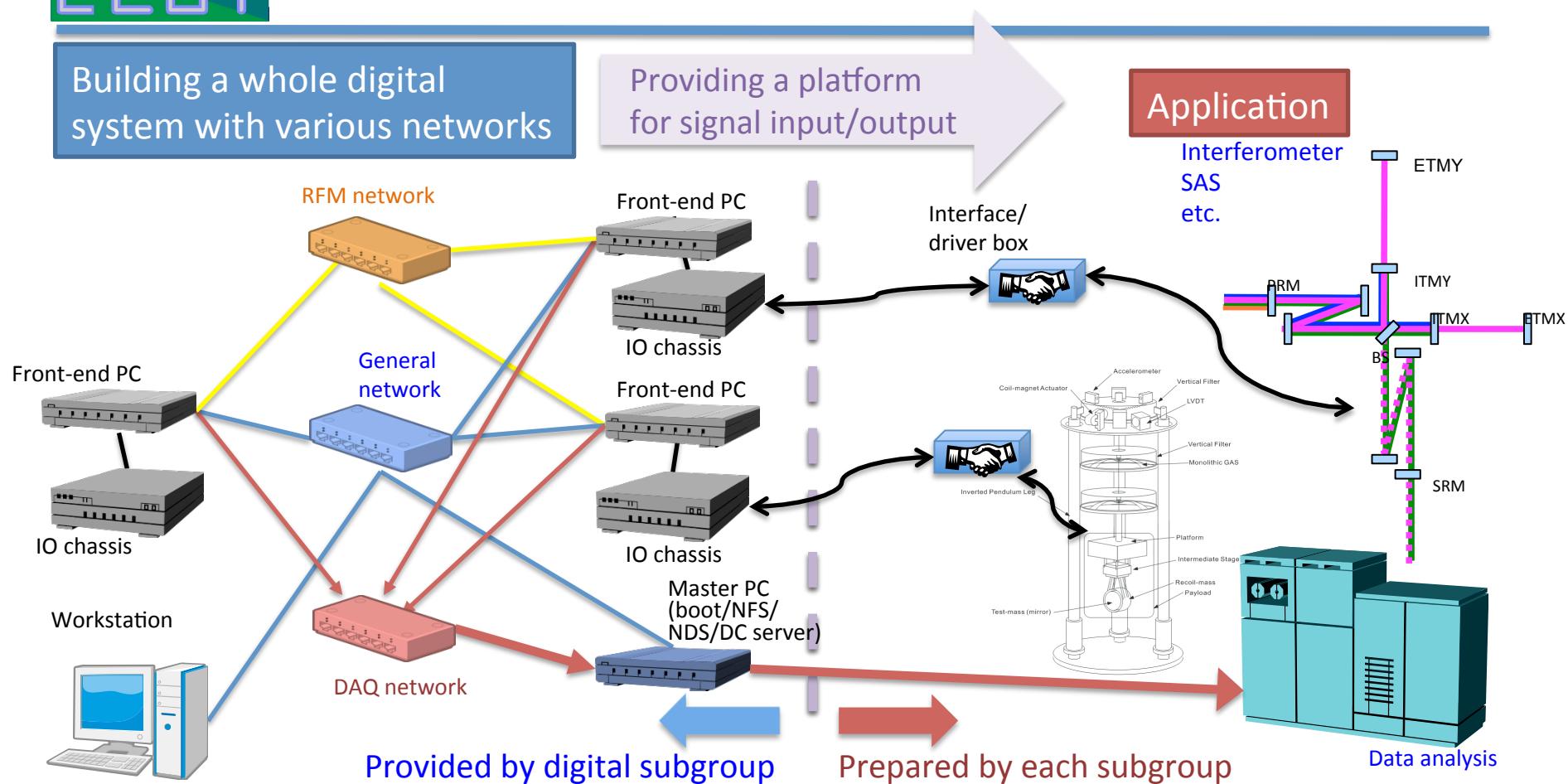
Definition from SEMP(JGW-M1100465):

In charge of development of digital system to provide a flexible human interface for a km scale interferometer to all subsystems for controls, monitors, switches and diagnoses.

1. Function as **Real time control**
 - For complicated multiple DOFs
2. Function as **Data acquisition system** for GW waves
 - Control signal = GW data
3. Function as **IFO tuning system**
 - Reducing time for improving sensitivity
4. Function as **Automatic IFO operation**
 - Stable observation
5. Function as **information collecting system** for IFO
 - Automatic channel assignment for huge number of channels

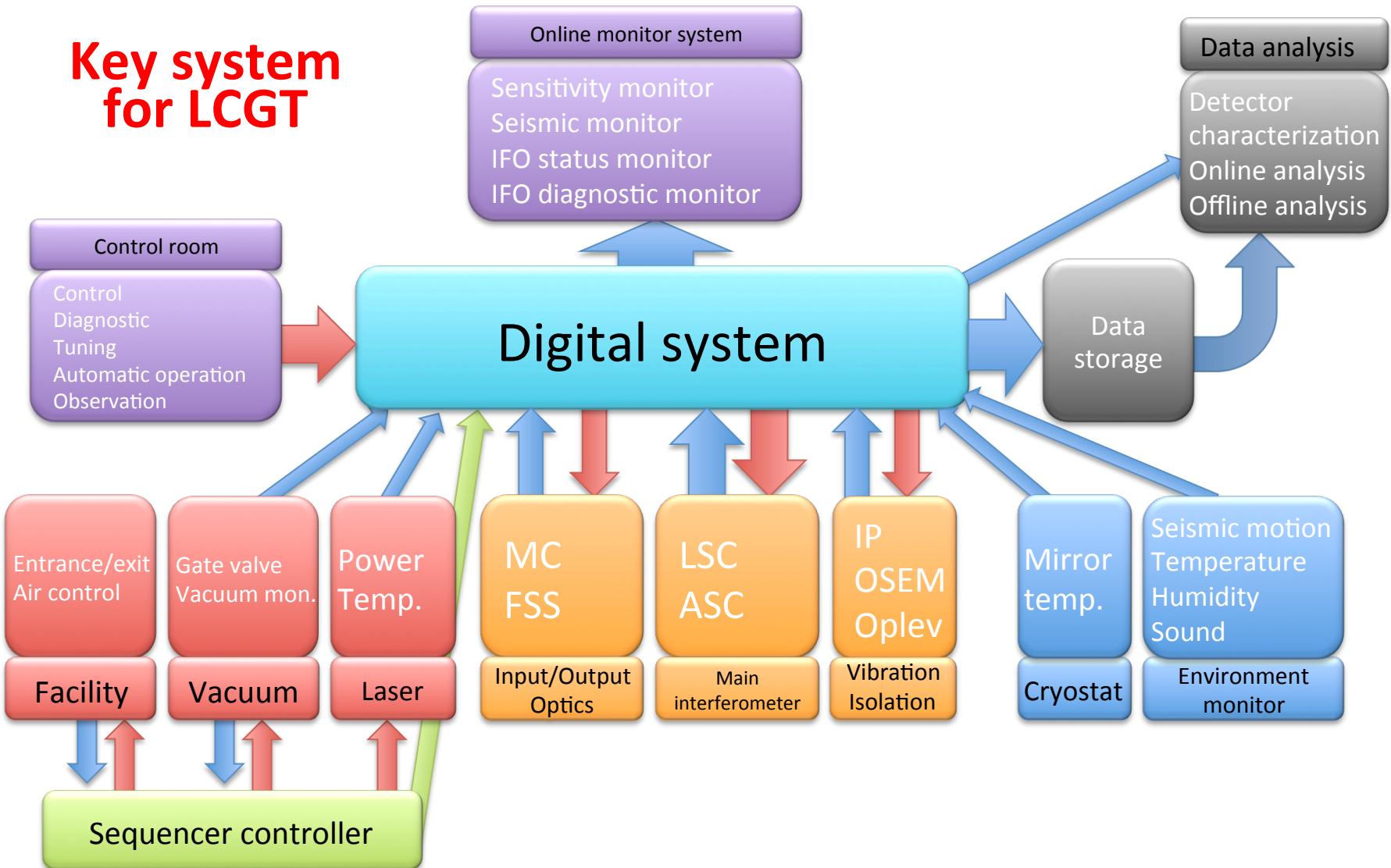


1-1. Definition and scope of the subsystem (cont'd)



- Real time system
- PC, software
- ADC/DAC/BO, AA/AI
- DAQ RFM/timing network
- Control, monitor, switch
- Auto lock, auto alignment
- Commissioning, noise hunting
- Diagnosis, tuning, calibration
- Operation, observation

1-2. Important interface





1-2. Important interface: to each subgroup

- FCL: network infrastructure, isolated room, entrance/exit system, monitors in control room
- VAC: vacuum monitor, Gate valve switch -> channel list, connector shape, EPICS interface
- VIS: OSEM, oplev, stepper/pico motor -> channel list, connector shape, variable gain amp, whitening/dewhitening, stepper/pico motor driver
- CRY: temperature monitor, switch for cryostat -> channel list, connector shape, EPICS interface
- MIF: IFO control for LSC and ASC, switch for common mode servo, tuning, diagnostic, auto lock, auto alignment, calibration, online monitor, operation, observation -> channel list, connector shape
- AEL: PD signal (DC), QPD signal (DC), I & Q servo output signal, switches for circuits, DC power supply monitor, DC power supply, cable, connector, AA/AI filter, VGA, whitening/dewhitening -> channel list, connector shape



1-2. Important interface: to each subgroup(cont'd)

- IOO: switch for for PMC, FSS, MC, OMC servo, FSS temp. control, control for MC and OMC, modulation depth controller, pico motor for steering mirror, pico motor for circulator-> channel list, connector shape, pico motor driver
- LAS: power/temperature monitor, thermal control, inter lock -> channel list, connector shape, EPICS interface
- GIF: physical environment monitor -> channel list, connector shape
- DAT: frame data, online analysis, calibration, data rate
- AUX: Oplev, picomotor for steering mirror, CCD monitor switch -> channel list, connector shape, EPICS interface

Digital system is a platform to realize above functions. Each functions should be implemented by each subgroup.



1-3. Design phase: Pending items

Not many

- Slow EPICS controller
- Simulated plant



2-1. Target specification

Global requirements

- Observation bandwidth
 $>5\text{kHz}$
- Dynamic range $>120\text{dB}$
- Control bandwidth $>200\text{Hz}$
- Number of channels >1024
- Number of output channels
 >256

Internal requirements

Item	Requirements	Comment
Sampling rate	$\geq 16384\text{Hz}$	65536Hz at ADC, then decimated to 16384Hz
ADC bit resolution	$\geq 16\text{bit}$	
Dynamic range of input	$\geq +/-15\text{V}$	Differential input
Dynamic range of output	$\geq +/-10\text{V}$	Differential output
ADC noise	$<3\mu\text{V}/\text{rHz}$	Effectively reduced by whitening filter
DAC noise	$<3\mu\text{V}/\text{rHz}$	Effectively reduced by dewhitening filter
time delay	$<100\text{usec}$	For $>200\text{Hz}$ UGF
Input channel numbers	$>2048\text{ch}$	(16kHz: $>128\text{ch}$, 2kHz: $>512\text{ch}$, 64Hz: $>1024\text{ch}$)
Output channel numbers	$>512\text{ch}$	For mirrors, seismic attenuators, PZTs etc.
Stored channel numbers	16kHz: $>64\text{ch}$, 2kHz: $>512\text{ch}$, 64Hz: $>1024\text{ch}$, 16Hz: $>10000\text{ch}$	$\sim 300\text{TB/year}$

Provides a robust and flexible platform to IFO and all subsystems
for **control, monitor, diagnostic, switch**
during **installation, commissioning, operation, observation**



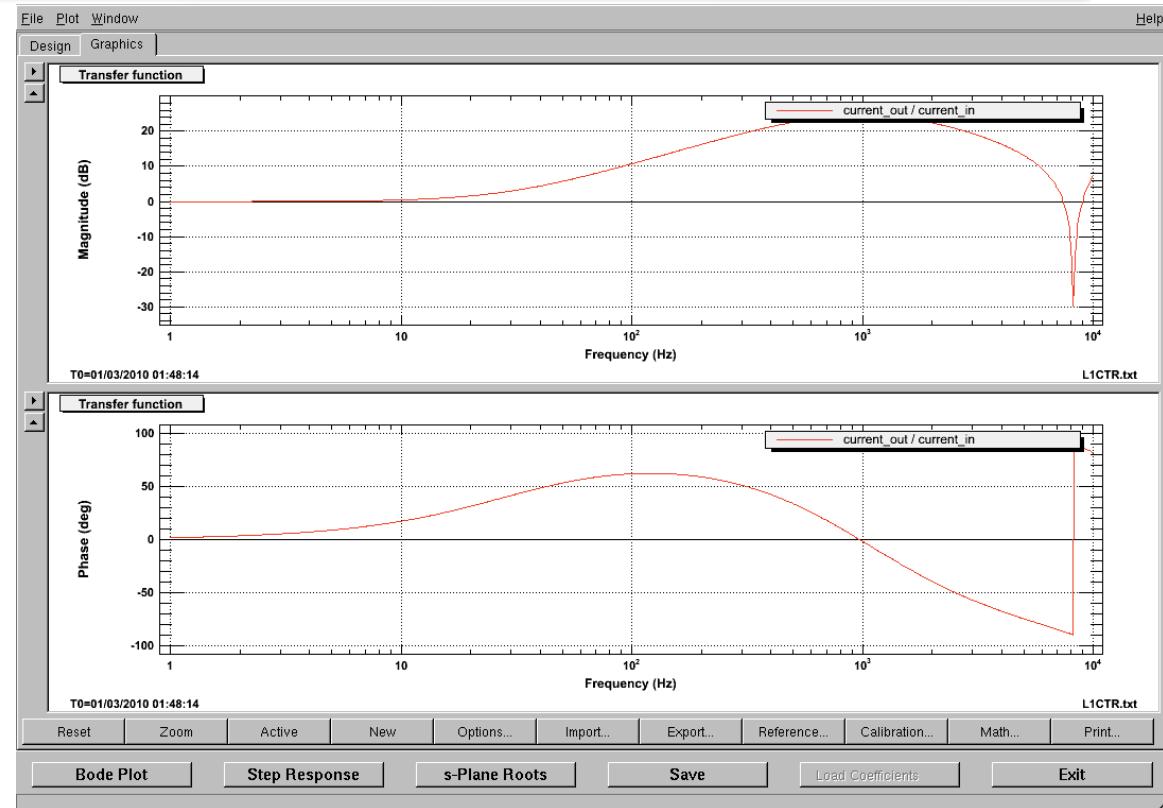
2-1. Target specification: hardware

1. Dual x86 processors, with four CPU cores each.
2. Processor clock speed of ~3GHz.
3. Minimum 8 Gigabyte of memory.
4. Two Gigabit Ethernet interfaces.
 - General TCP/IP
 - DAQ network by Myrinet or Open-MX protocol
5. One, or more, real-time network interfaces
 - Reflected Memory (RFM)
 - PCI Express (PCIe) network interface
6. A PCIe interface to the PCIe expansion chassis with a maximum of 10 PCIe cards installed.



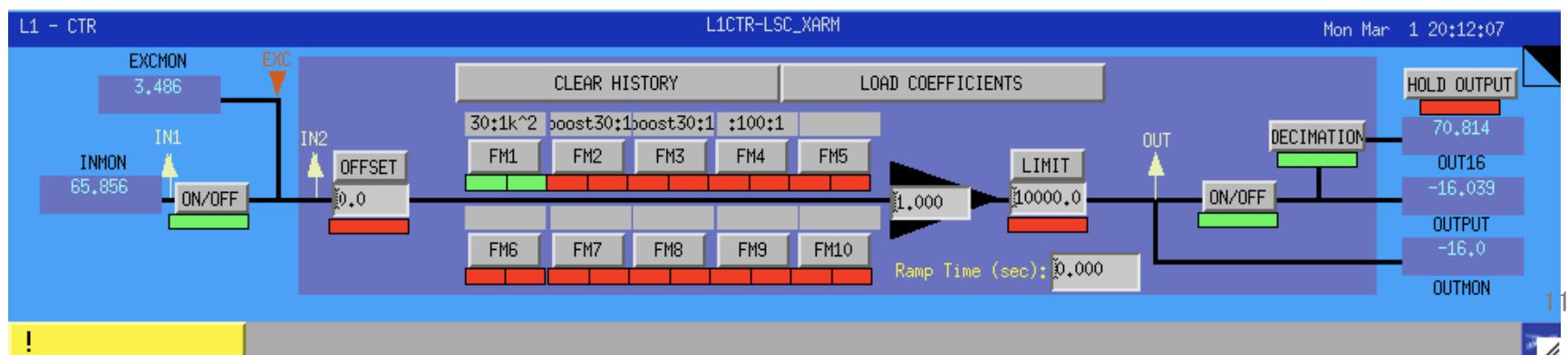
2-1. Target specification: software

- Dataviewer: oscilloscope,
- DTT: FFT analyzer
- Foton: digital filter composer
- Ezcademod: digital modulator/ demodulator
- Foton: GUI digital filter composer

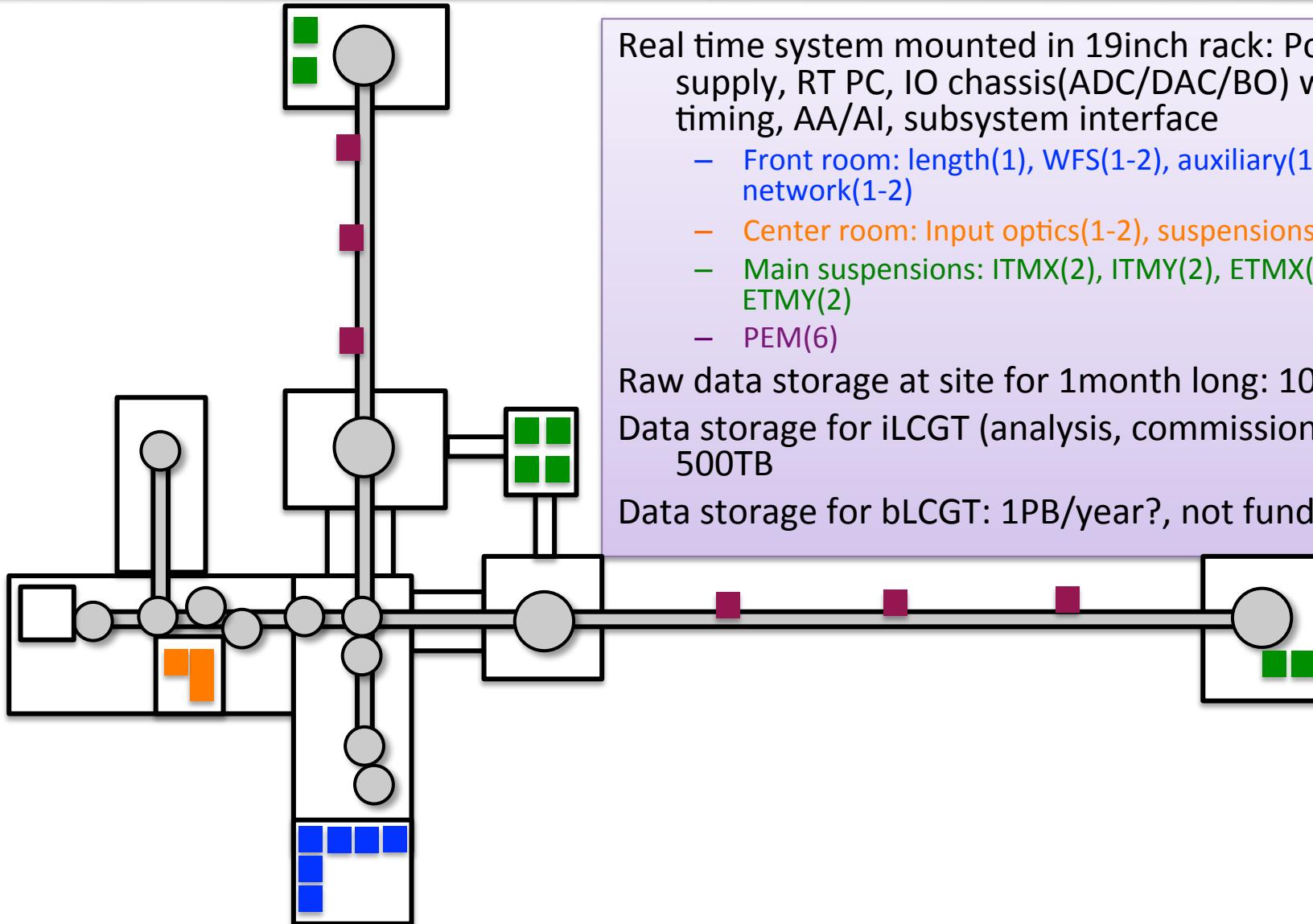


Filters on MEDM

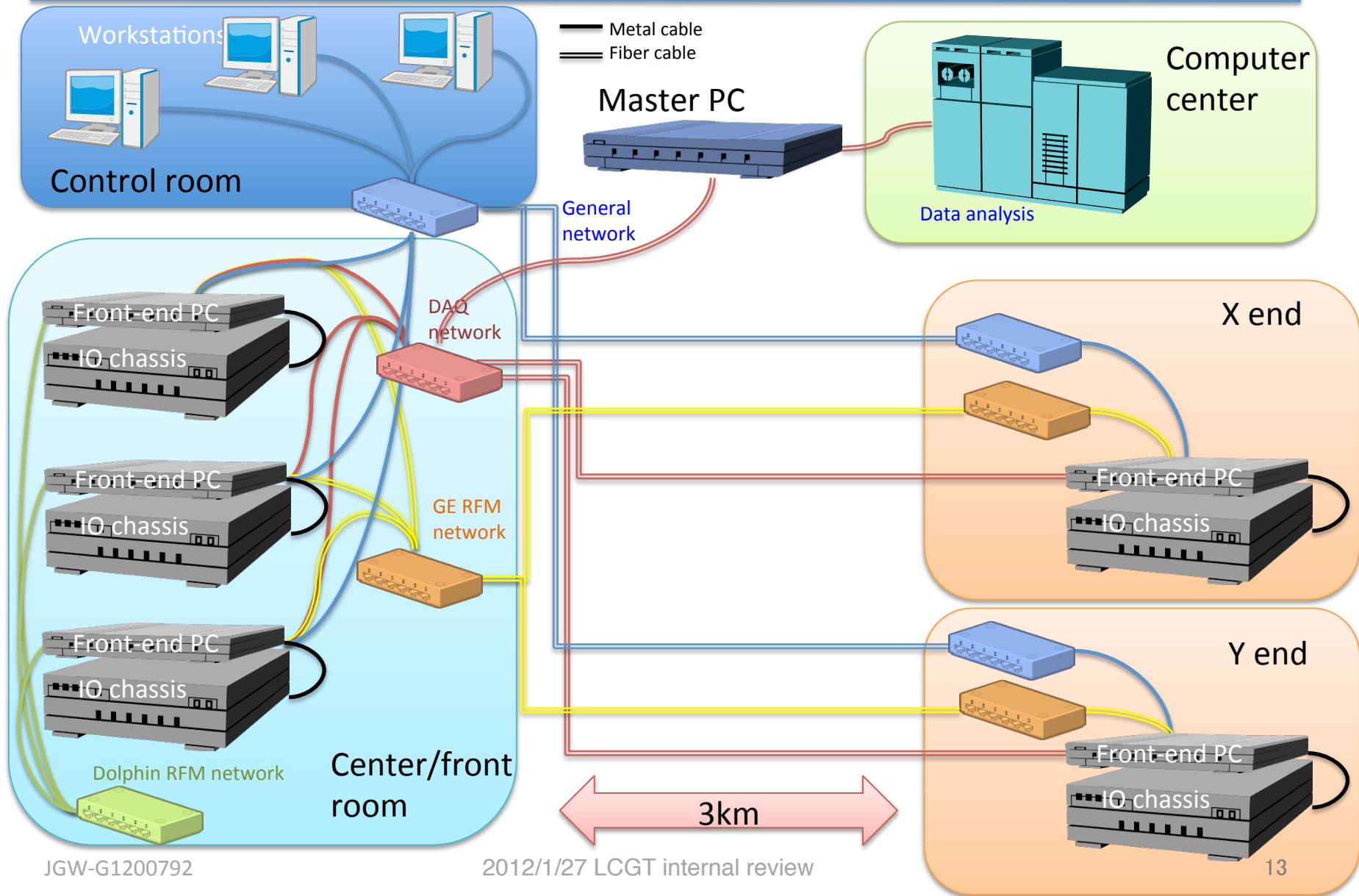
- Signal excitation
- 10 filter banks
- 3 monitor point IN1/IN2/OUT



2-2. Final design: RT rack position

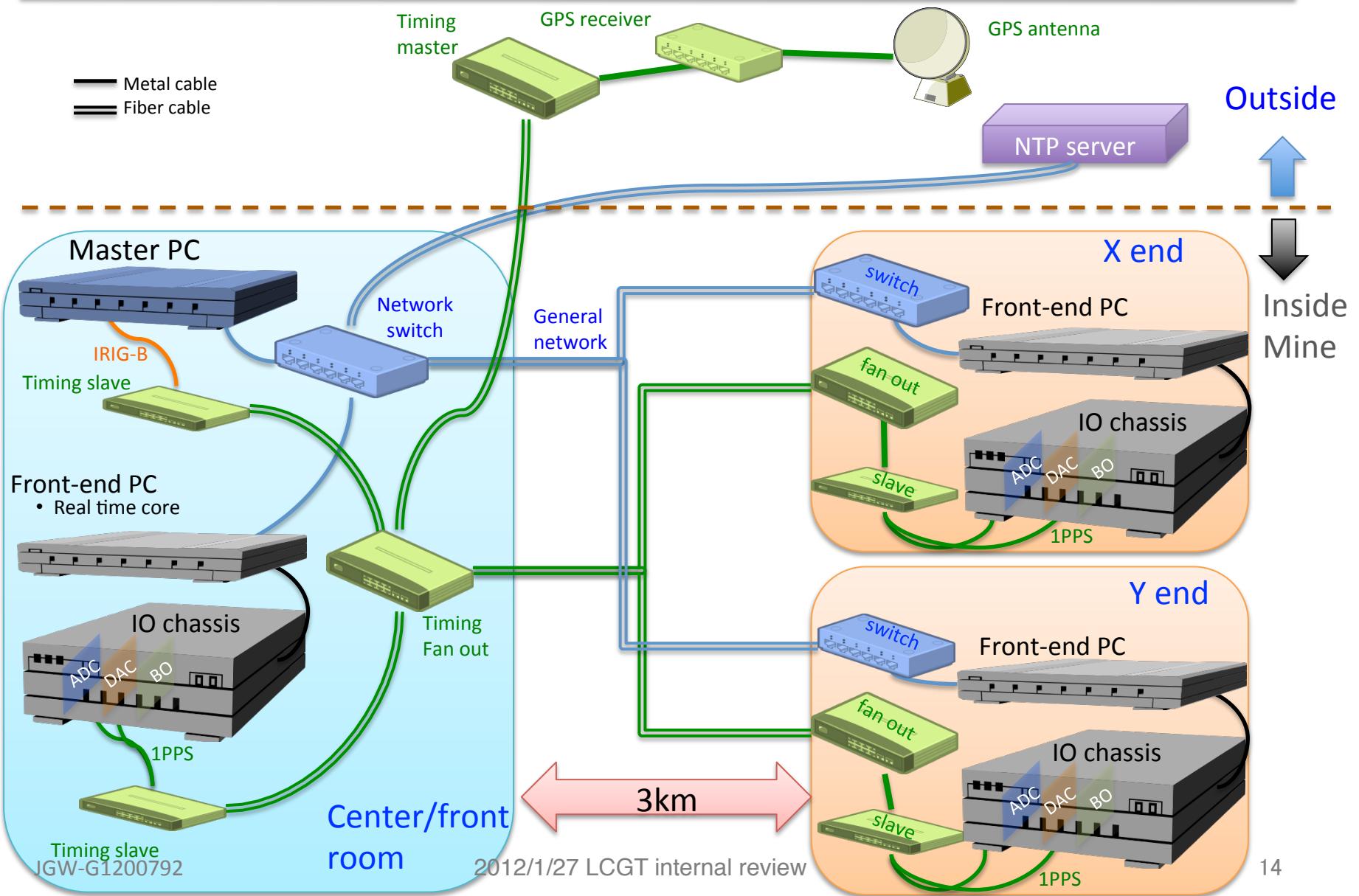


2-2. Final design: Network design



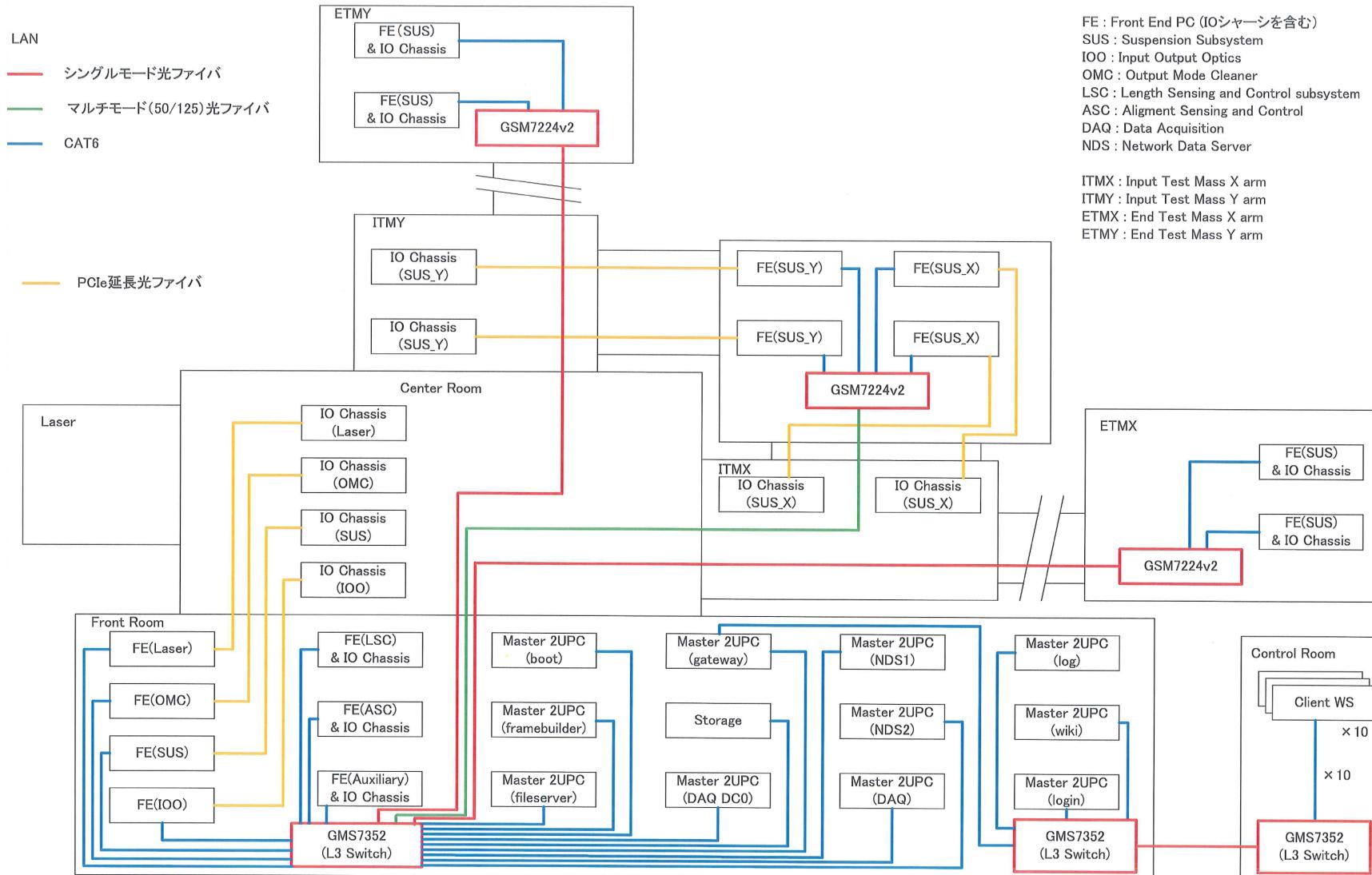


2-2. Final design: Timing Network



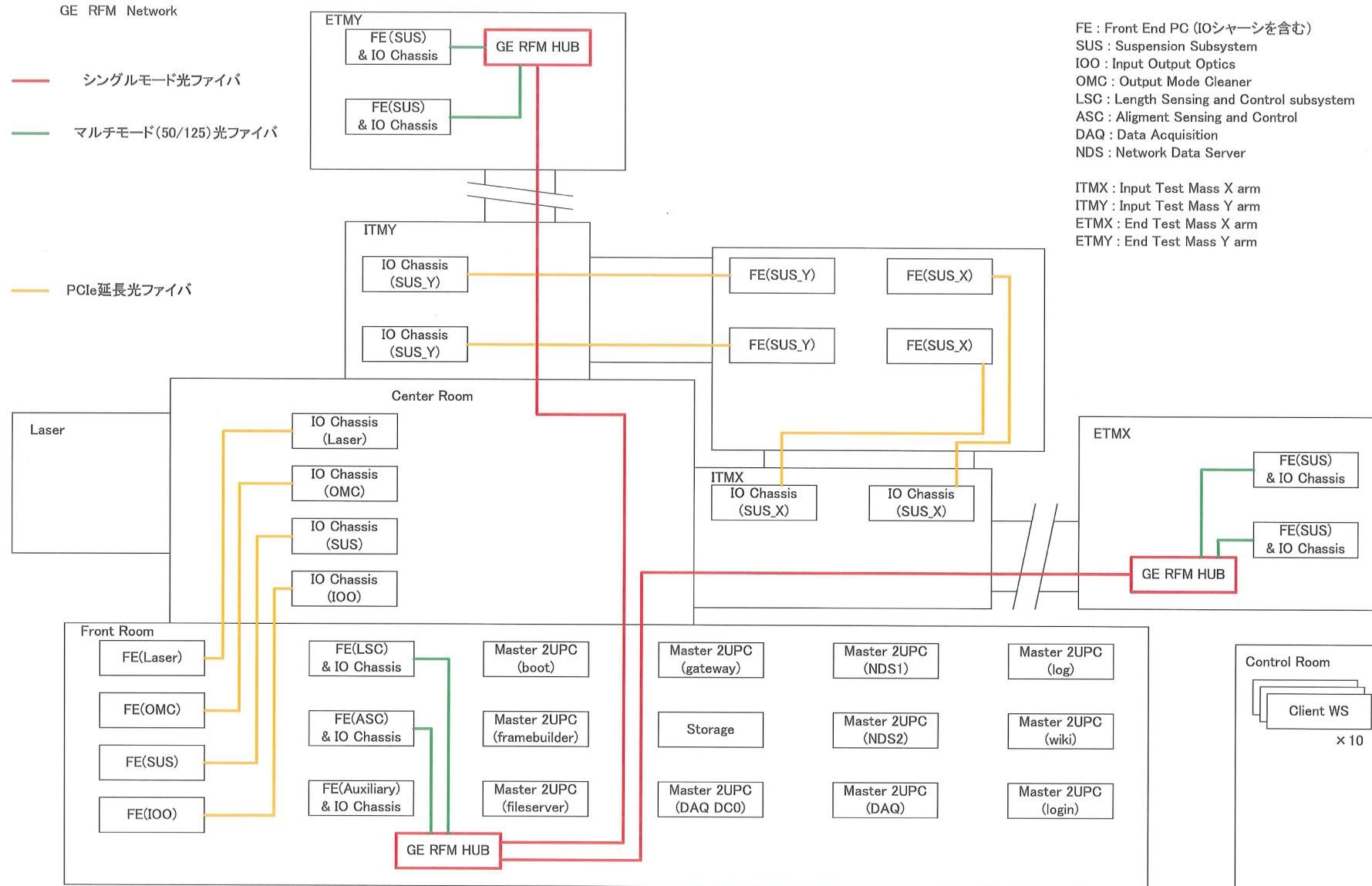


General network diagram



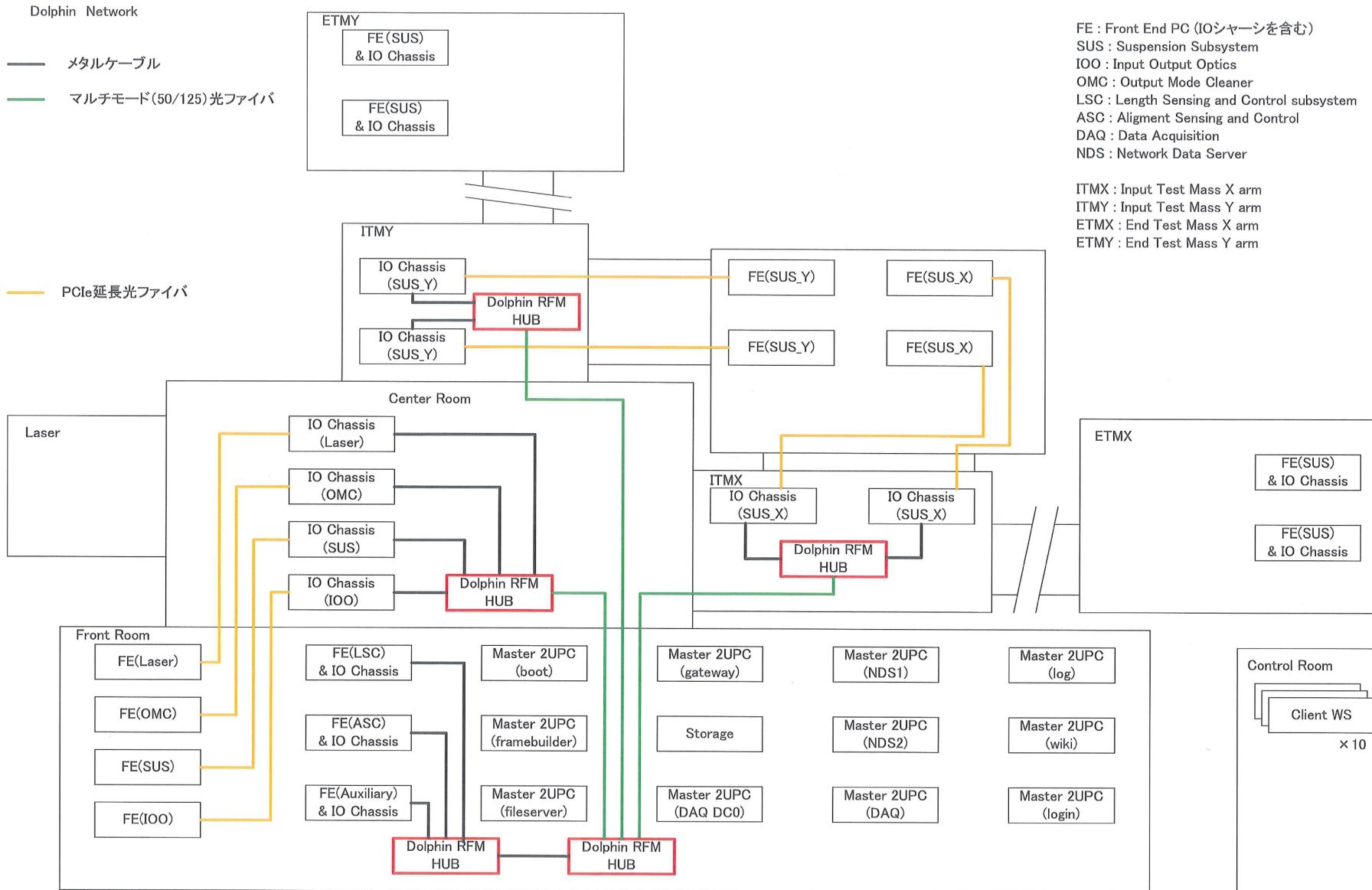


GE reflective memory network diagram



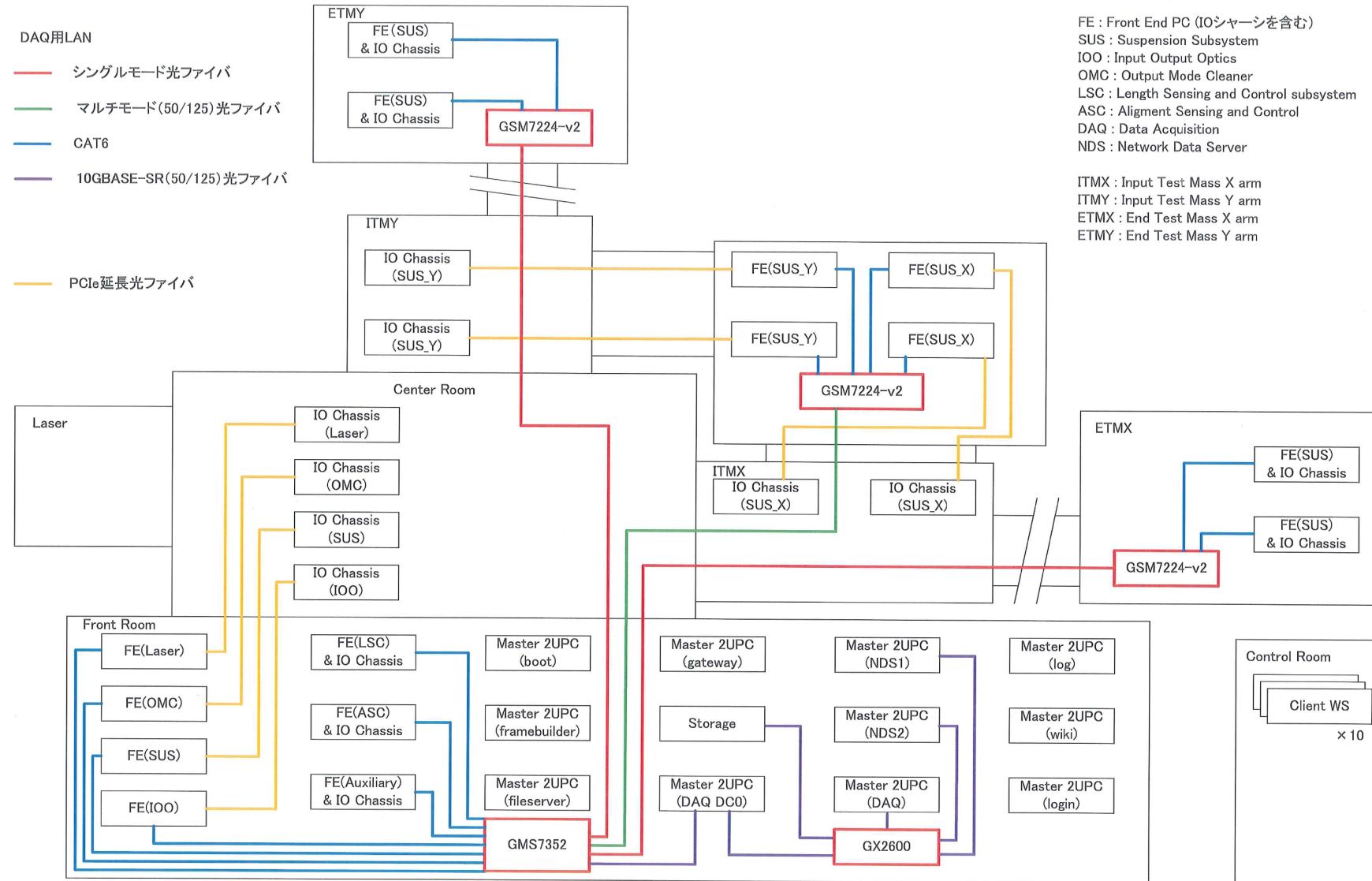


Dolphin reflective memory network diagram





DAQ network diagram

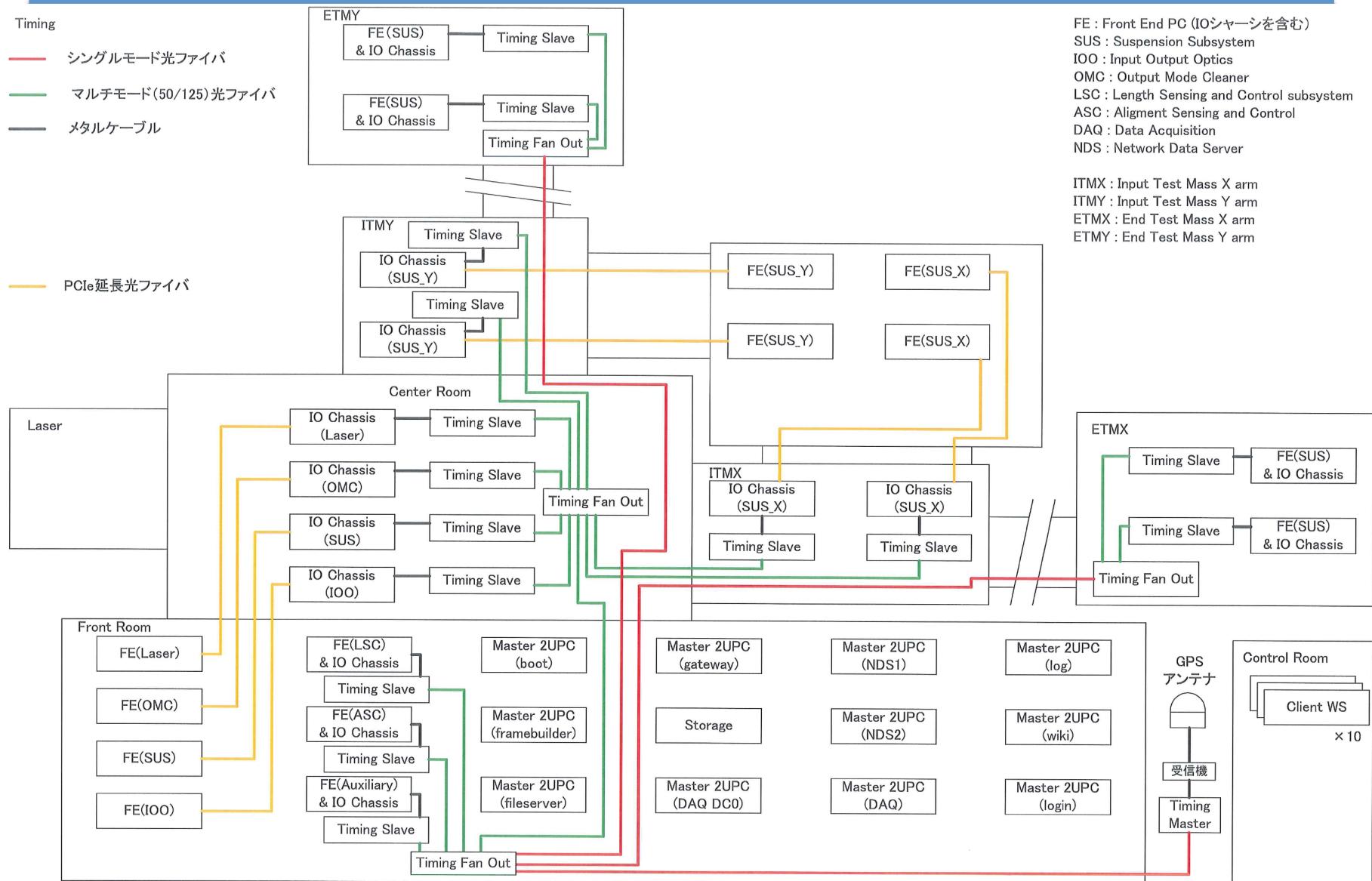




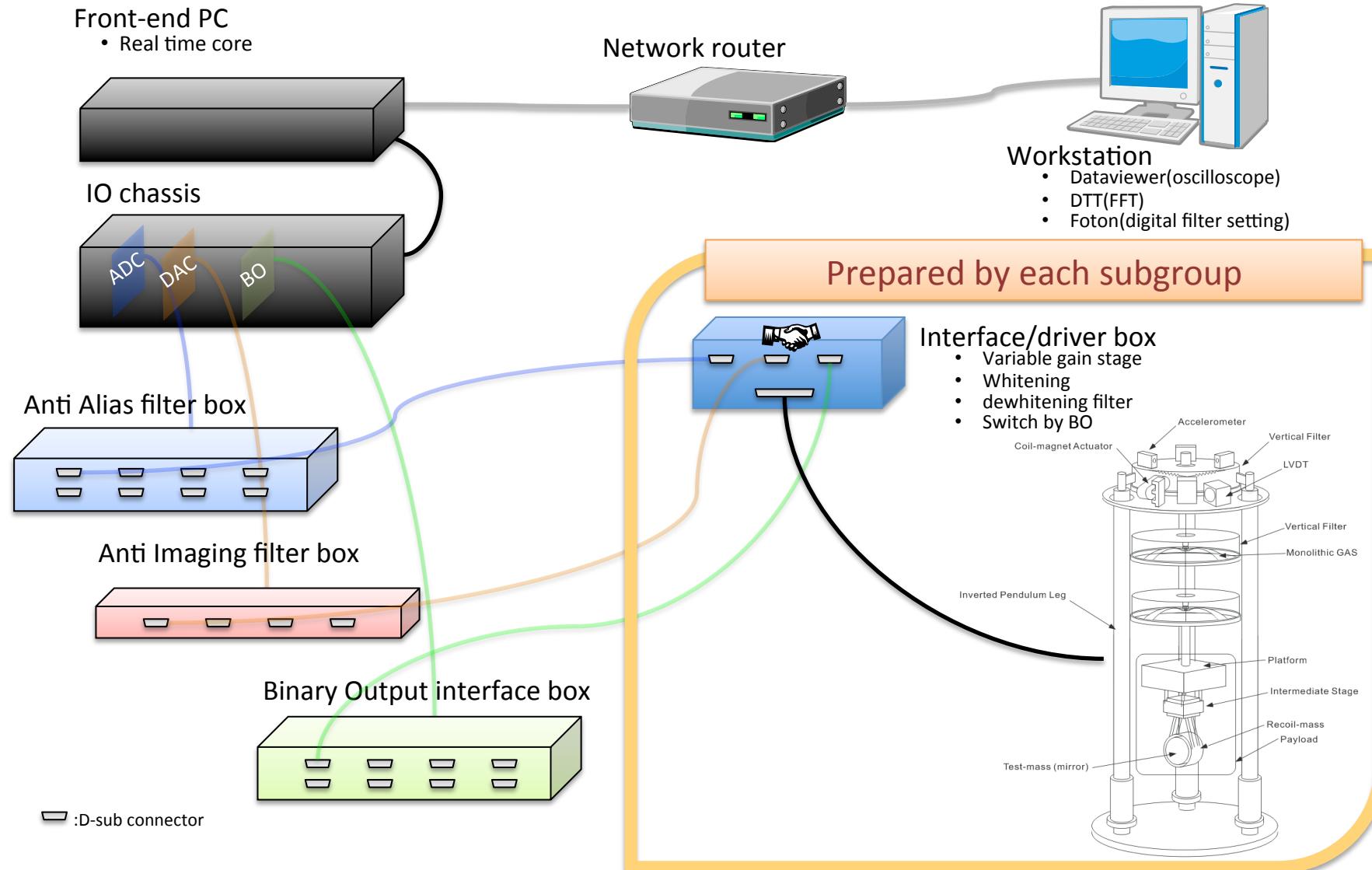
Timing network diagram

Timing

- シングルモード光ファイバ
- マルチモード(50/125)光ファイバ
- メタルケーブル
- PCIe延長光ファイバ



2-2. Final design: Connecting to subsystems





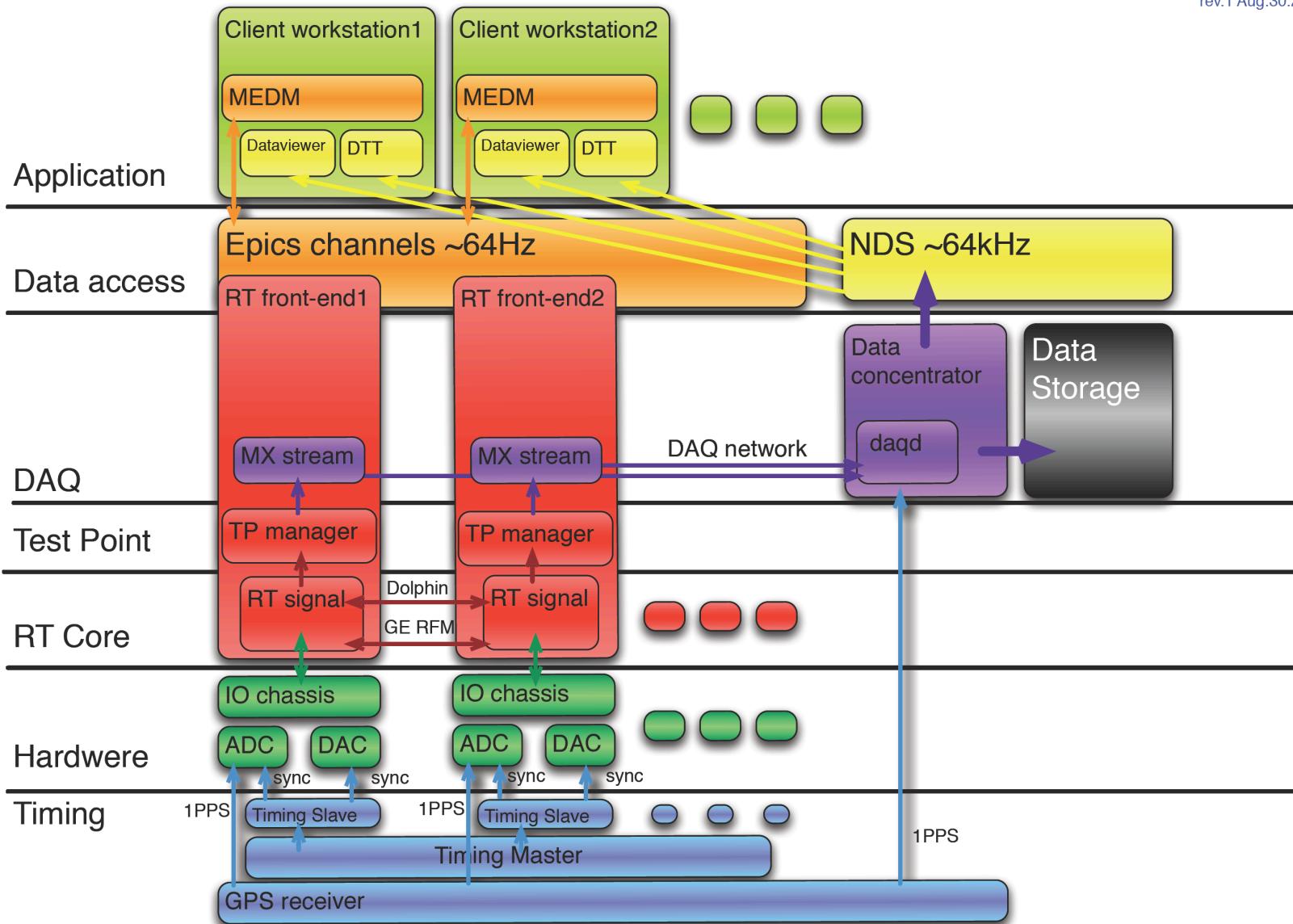
2-2. Final design: Interface

- ADC 32ch/card
 - 16kHz sampling
 - With Anti Alias filters
 - 2uV/rHz
 - D-sub 9pin(for 4ch, differential), +/-20V input
- DAC 16ch/card
 - With Anti Imaging filers
 - 1.5uV/rHz
 - D-sub 9pin(for 4ch, differential), +/-10V output
- BO 32ch/card
 - D-sub 9pin(for 4ch, differential), 0 or +5V output
 - Ex. Variable gain amp for 16 steps/1 D-sub connector
- Pico/stepping motor controller using slow EPICS

Note: D-sub 37pin may be supported for all input/output

LCGT Digital System Layer Map

JGW-D1100588
rev.1 Aug.30.2011





Slow EPICS system for Physical Environmental Monitors

- Agreed to use RT system as PEM DAQ
 - Current RT system can be used since fiber cables exist every 500m in the arm

- Needs pico motor controller
 - tested at CLIO, but using single PC

- Multiple PCs for Pico/stepping motor and PEM
 - Another PCs at each vacuum chamber?



Making channel lists

- Needs channel list for ADC/DAC/BO
 - ADC input ~2048ch
 - will be categorized as class1(IFO main), class2(IFO sub), class3(PEM, physical environment monitor)...
 - DAC output: ~512ch
 - BO: ~2048ch
- DAQ channel: stored signals to data storage as 16kHz, 2kHz, 64Hz...



DAQ Channel list

	Number of stored channels	Data acquisition, Data analysis, IFO control 16kHz:64ch, 2kHz:512ch, 64Hz:1024ch 16Hz:16384 epics channels (see channel list)
*	Data bit resolution at ADC/DAC	Data acquisition 16bit = 65536
*	Data bit resolution in PC	Data acquisition 32bit = 4 Byte integer
	Data transfer rate	Data acquisition 4MB/sec for 16kHz, 4MB/sec for 2kHz, 128kB/sec for 64Hz, 1MB/sec for 16Hz, Total ~10MB/sec ~30GB/hour ~1TB/day ~300TB/year

6. Channel list

a. 16kHz (total 64ch)

Part	Channel point	Channel number	Description
Laser	Output laser power[W]	1	
	IFO Input laser power[W]	1	
MC	REFL	1	
	MC length feedback	1	
	MC frequency feedback	1	
LSC	I&Q dor DARM, CARM, MICH, PRC, SRC, etc.	10	
	error, feedback	10	
SUS	length * 10 suspensions	10	

b. 2kHz (total 256ch)

Part	Channel point	Channel number	Description
ASC	WFS	5xpitch, yaw=50	
	Oplev	10xpitch,yaw=100	

c. 64Hz Long term monitor (total 512ch)

Part	Channel point	Channel number	Description
Temperature[deg]	room	10	center, end, arm
	table	10	laser, REFL, AS, pickoff, end
	suspensions	50	Low temperature
	mirrors	50	Low temperature
Humidity[%]	rooms	10	center, end, arm
Dust	rooms	10	center, end, arm
Laser	crystal temperature[degree] and etc.	10	
	Master laser power[W]	2	



2.3 Schedule

- Schedule update due to 1 year delay
 1. Prototype test on CLIO
 2. Standalone system for subsystems
 3. Small network test with 2 or 3 PCs
 4. Large network test with ~20 PCs
 5. Installation

FY	2010	2011	2012	2013	2014	2015	2016									
Quarter	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
Main Phase	Design				Tunnel				Vacuum		FPMI		RSE			
Prototype test	CLIO operation	■	■	■												
	Data analysys test				■	■	■									
Standalone system for subsystems	Hard/software setup		■	■	■											
	Circuit				■											
	Delivery					■	■	■								
Article test	Small network			■	■											
	Large network system				■	■	■	■								
	Circuit				■	■	■									
	Inspection					■	■	■								
Full system	Installation								■	■	■	■				
	Tuning											■				
Upgrade	RSE											■	■	■		
	Cryo											■	■			



2.4 Quality assurance: Continuous upgrading the digital system

- 2009 Feb.~ @Caltech
 - First prototype standalone construction using old (Windriver) aLIGO type digital system
- 2009-2010 prototype full test @ CLIO
- 2010 Dec.-Jan. @Caltech
 - Upgrading to new (Gentoo) aLIGO type standalone digital system
- 2011 Jan. @LHO
 - Visiting LIGO LHO site to design whole network for digital system
- 2010 July @Kashiwa with Joe Betzweiser
 - Upgrading to network configuration using multiple RT PCs with RFM and DAQ network
 - Working with 1PPS timing system



2.4 Quality assurance (cont'd)

- A. 2009-2010 prototype test @ CLIO
 - Basic IFO operation and noise performance
- B. 2011- standalone system for subsystem
 - Data analysis, VIS, (IOO, CRY...)
- C. Small network test with 1 master and 2 RT PCs
 - GE RFM, Dolphin RFM, DAQ, timing network
- D. Full test@ Kamioka new facility
 - Many servers and constructing RT rack modules



Installation into mine



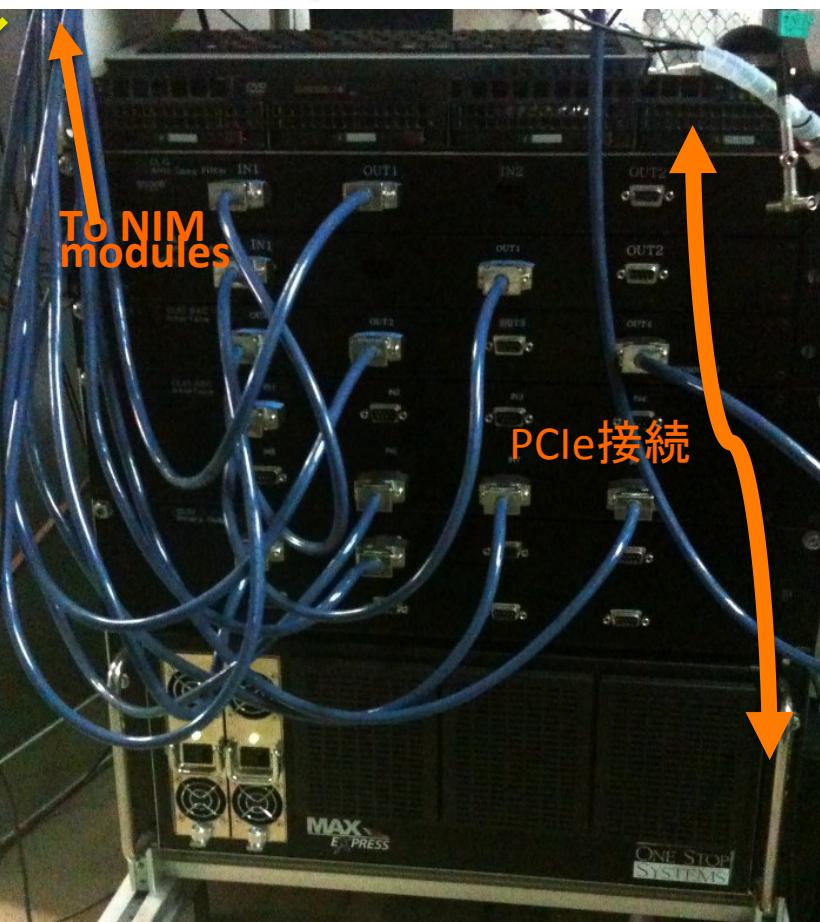
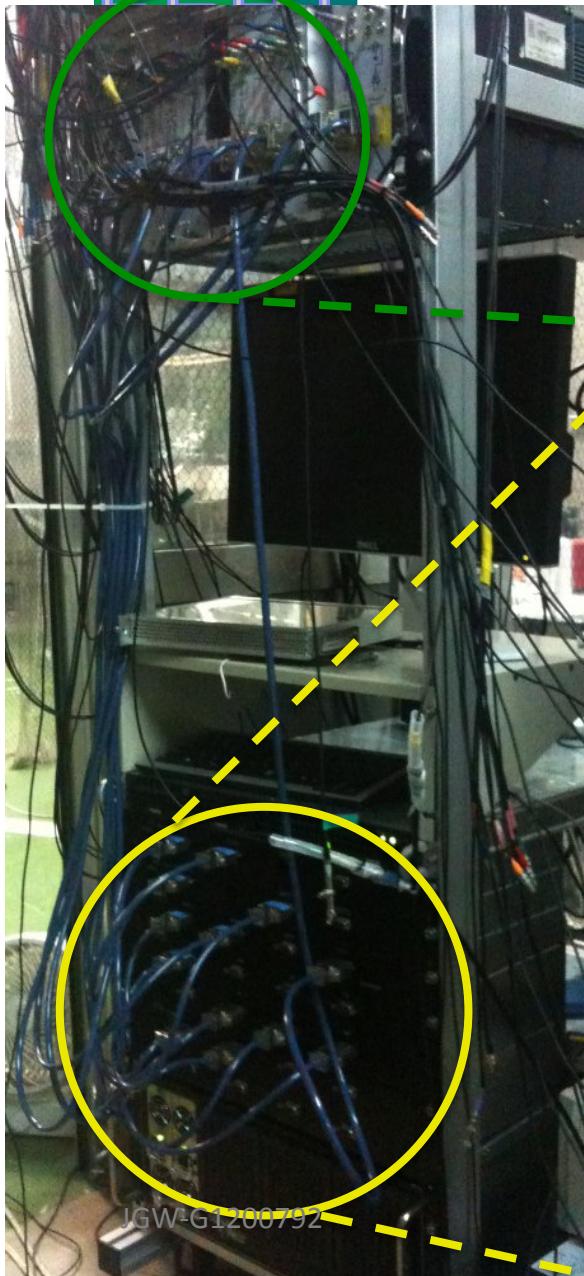
2.4 Quality assurance:

A. Prototype test @ CLIO

- Setting up Real-time control computers
 - Obtaining equipment in Japan like ADC/DAC/BO, IO chassis...
- Related analog circuits like AA/AI, WF/DWF
- Lock acquisition
 - linearizing error signal
 - normalizing power
- Calibration process on DTT
 - sensitivity monitor
- Noise performance
 - Switching WF/DWF by BO
- Auto alignment using Python based Pico motor controllers on EPICS
- Application for other R&D experiment



Pictures



Real time PC
CentOS 5.2+real time kernel
4core x 2 Xeon

Anti Imaging filters
Anti Alias filters

DAC adapter

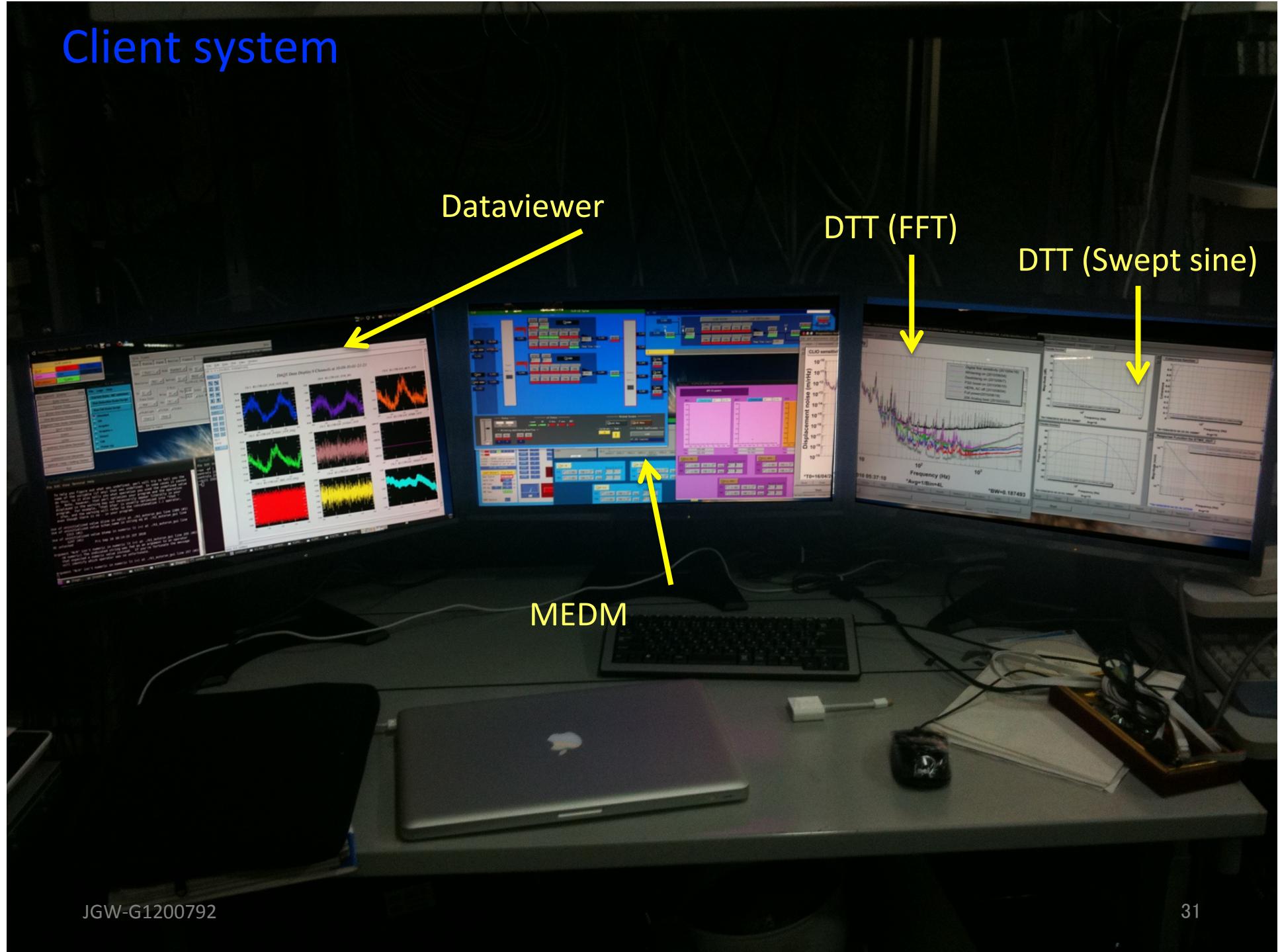
ADC adapter

Binary output adapter

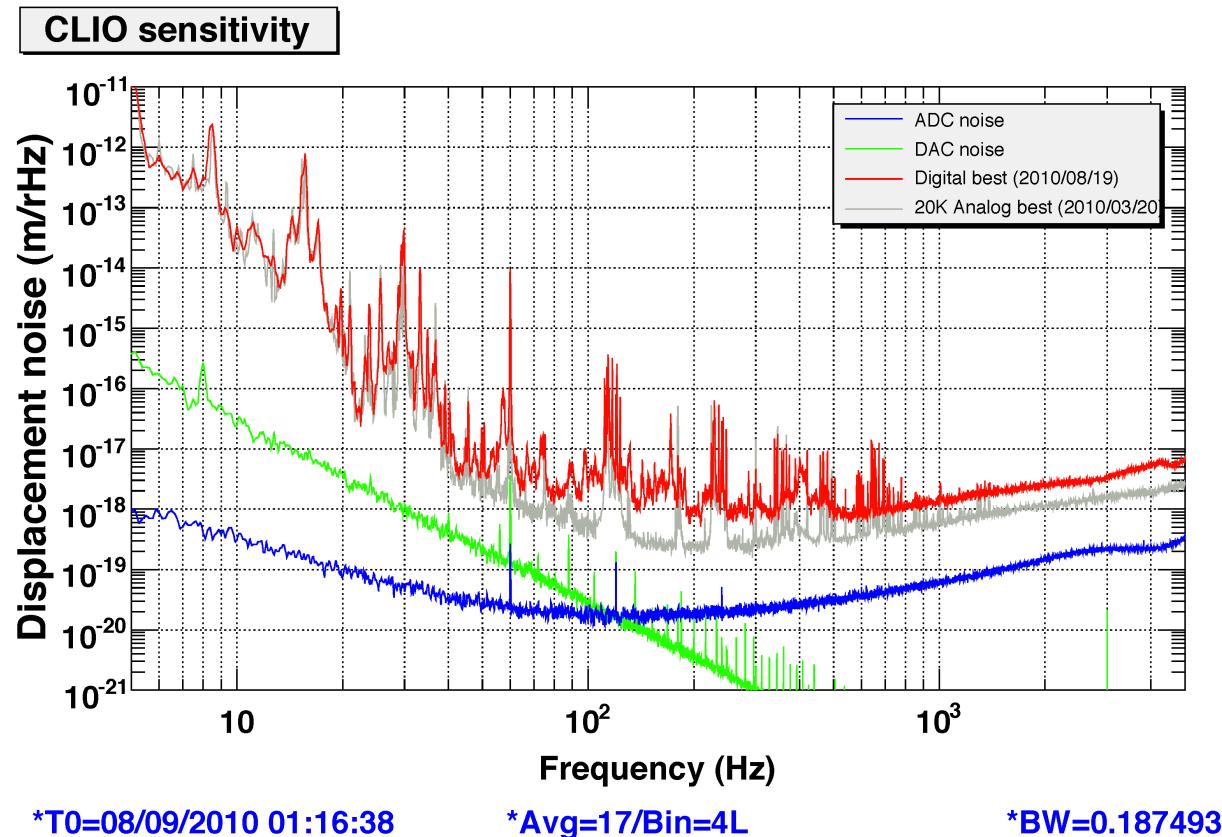
ADC/DAC
In Expansion Chassis

ADC:32ch/\$4K
DAC:16ch/\$3.5K
Binary Output:32ch/\$250

Client system



CLIO sensitivity using Digital control





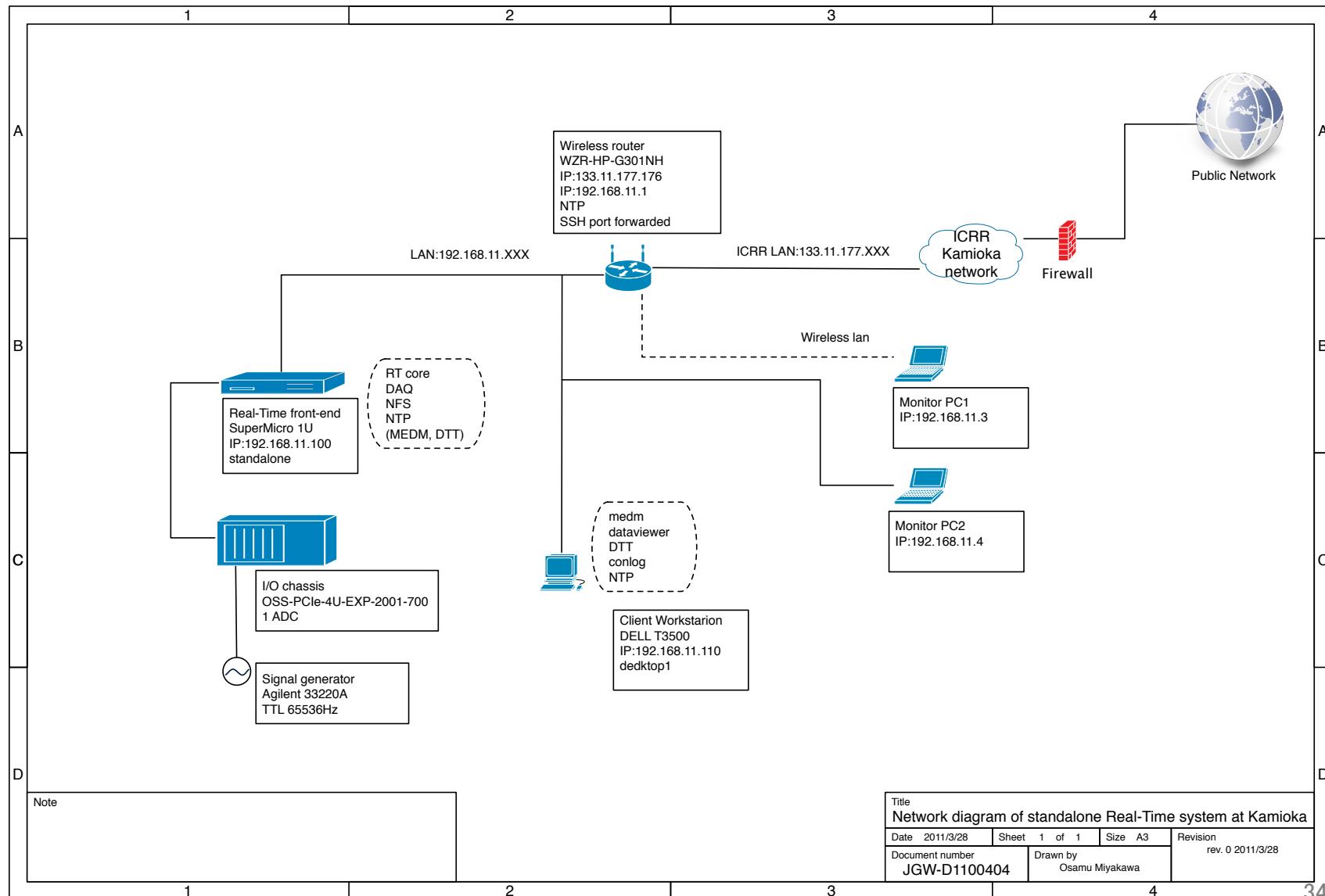
2.4 Quality assurance: B. Standalone system for subsystems

5sets of stand alone digital system will be delivered to subgroups in FY2011

1. Real time control computer as front-end
 2. Client workstation PC with software setup
 3. PCIe I/O chassis for ADC/DAC/BO modules
 4. Timing slave board
 5. ADC, DAC, Binary Output
 6. Anti Alias/Anti imaging filters
-
- good chance for subgroups to be accustomed with a digital system before the commissioning of LCGT

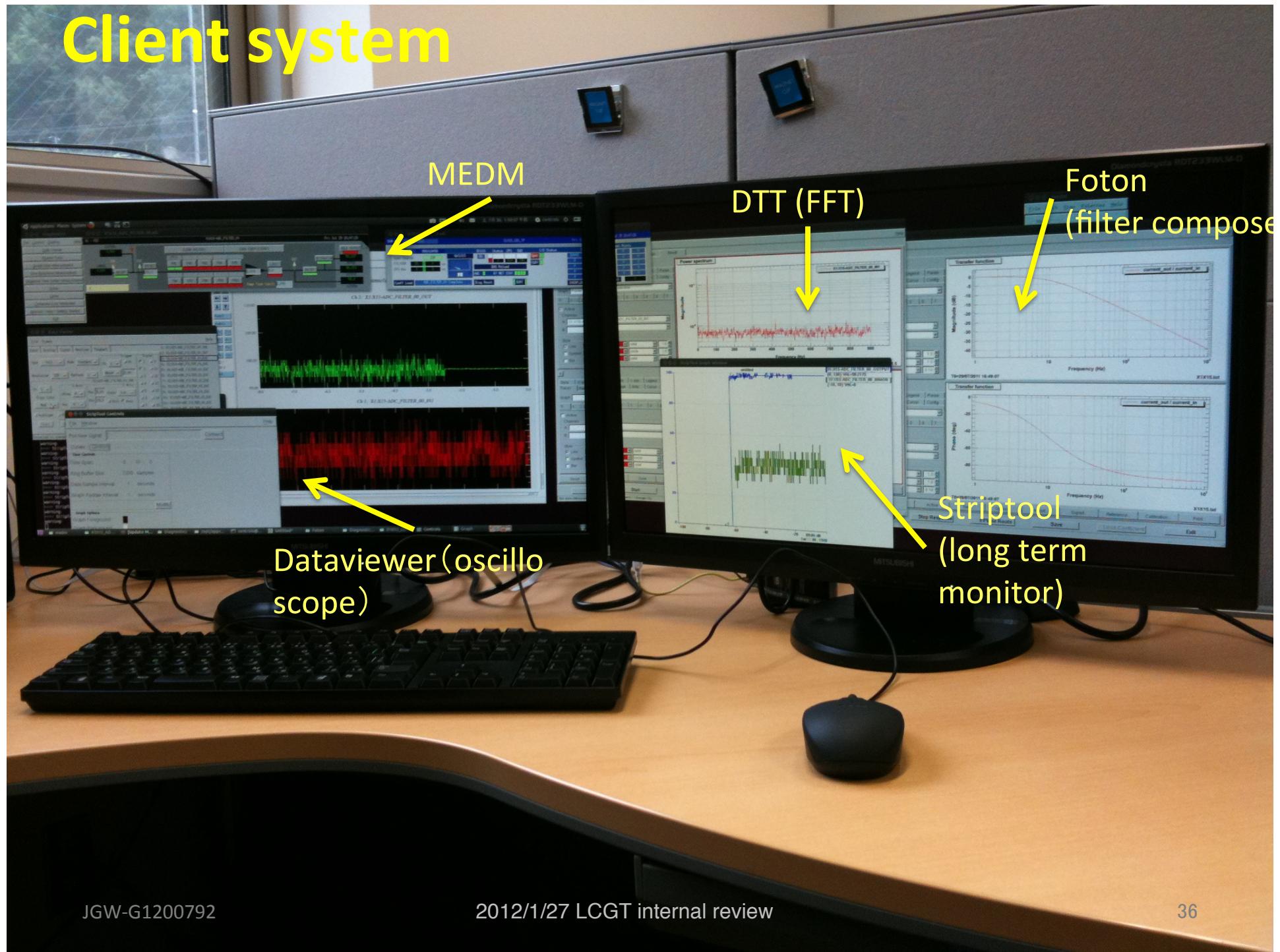


B. Standalone system for subsystems: Network diagram





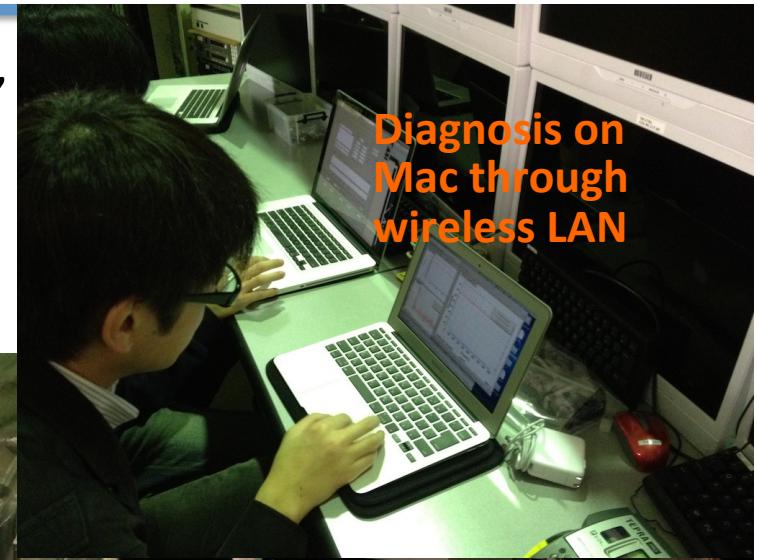
Client system





Delivering standalone digital system to NAO for online data analysis

- Simple standalone system (RT PC + ADC, Client WS, router) has been delivered to NAOJ on 12/6/2011.
- 3days work for installation, lecture and training
- Online analysis software will be developed by DAS group.



Preparation for mass production of circuits for DGS



- AA and AI for VIS are ready.
First control test will be performed in the next week.
- 6 AA and 6 AI will be made in this FY.



Ex. VIS channel list (preliminary)

Quantity matrix

	ADC	DAC	BO	Motor
LVDT	2	1		0
Geophone	1	0		0
Actualtor	1	1		0
Stepper Motor	0	0		1
OSEM	1	1		0

2 ADC, 2DAC / Type A
1ADC, 2DAC / Type B

Type A

4

	Qty.	ADC	DAC	BO	Motor
Pre Isolato	LVDT	4	8	4	0
	Geophone	4	4	0	0
	Actualtor	4	4	4	0
	Stepper Motor	4	0	0	4
	OSEM	0	0	0	0
GAS	LVDT	1	2	1	0
	Geophone	0	0	0	0
	Actualtor	1	1	1	0
	Stepper Motor	0	0	0	0
	OSEM	0	0	0	0
GAS	LVDT	1	2	1	0
	Geophone	0	0	0	0
	Actualtor	1	1	1	0
	Stepper Motor	0	0	0	0
	OSEM	0	0	0	0
GAS	LVDT	1	2	1	0
	Geophone	0	0	0	0
	Actualtor	1	1	1	0
	Stepper Motor	0	0	0	0
	OSEM	0	0	0	0
Pay load	LVDT	1	2	1	0
	Geophone	0	0	0	0
	Actualtor	1	1	1	0
	Stepper Motor	4	0	0	4
	OSEM	8	8	8	0
total		36	24	8	

Type B

7

	Qty.	ADC	DAC	BO	Motor
Pre Isolato	LVDT	4	8	4	0
	Geophone	4	4	0	0
	Actualtor	4	4	4	0
	Stepper Motor	4	0	0	4
	OSEM	0	0	0	0
GAS	LVDT	1	2	1	0
	Geophone	0	0	0	0
	Actualtor	1	1	1	0
	Stepper Motor	0	0	0	0
	OSEM	0	0	0	0
Pay load	LVDT	1	2	1	0
	Geophone	0	0	0	0
	Actualtor	1	1	1	0
	Stepper Motor	4	0	0	4
	OSEM	8	8	8	0
total			30	20	8

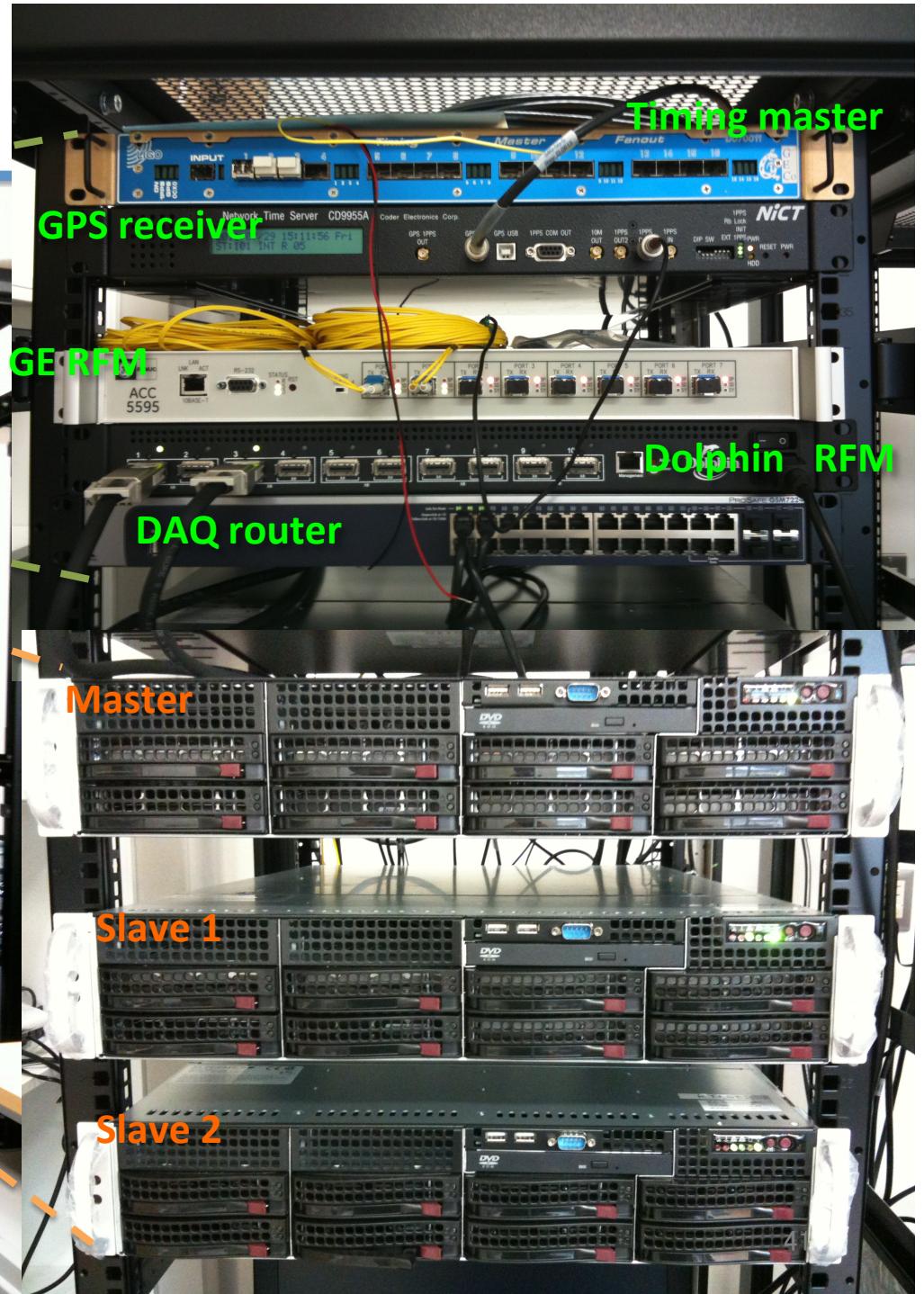
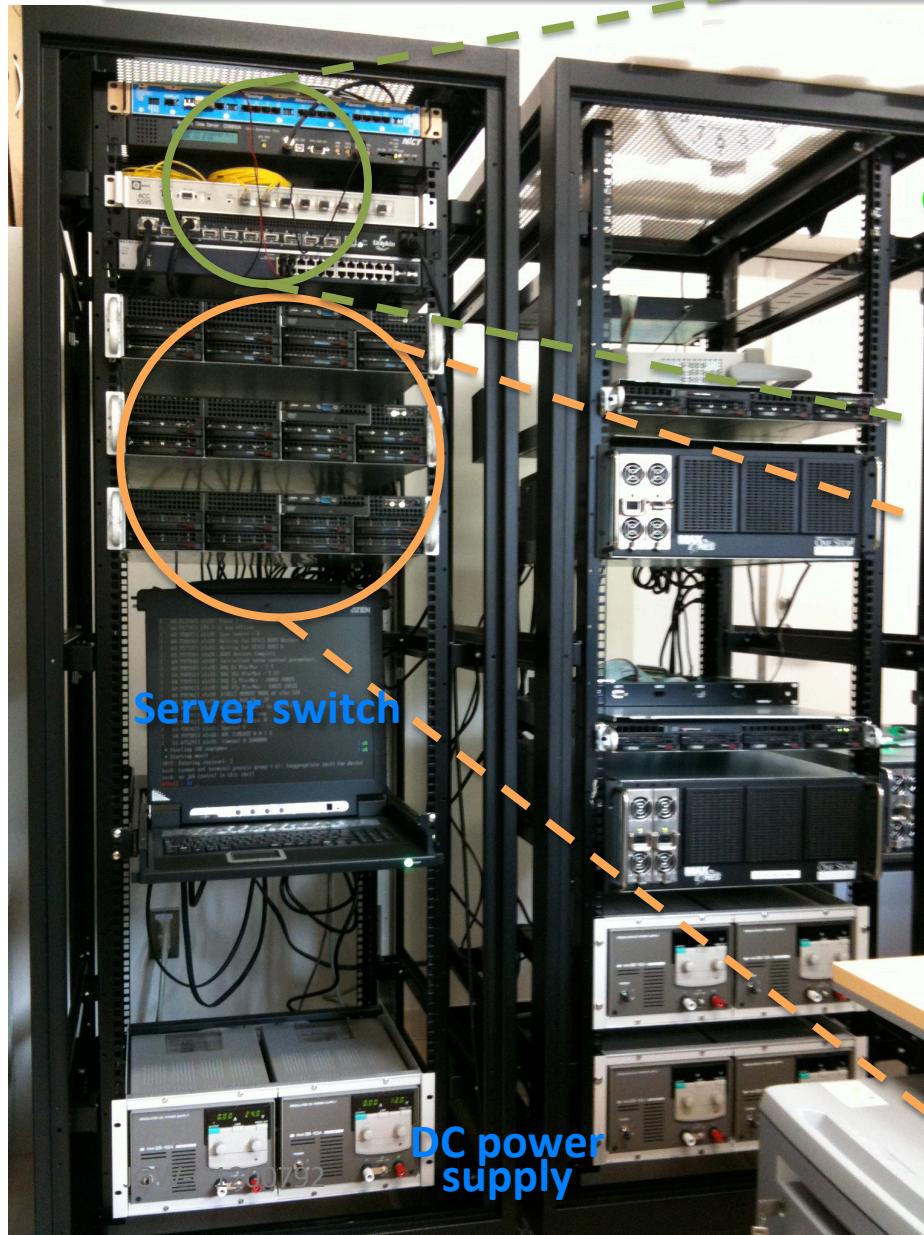


Other subgroups?

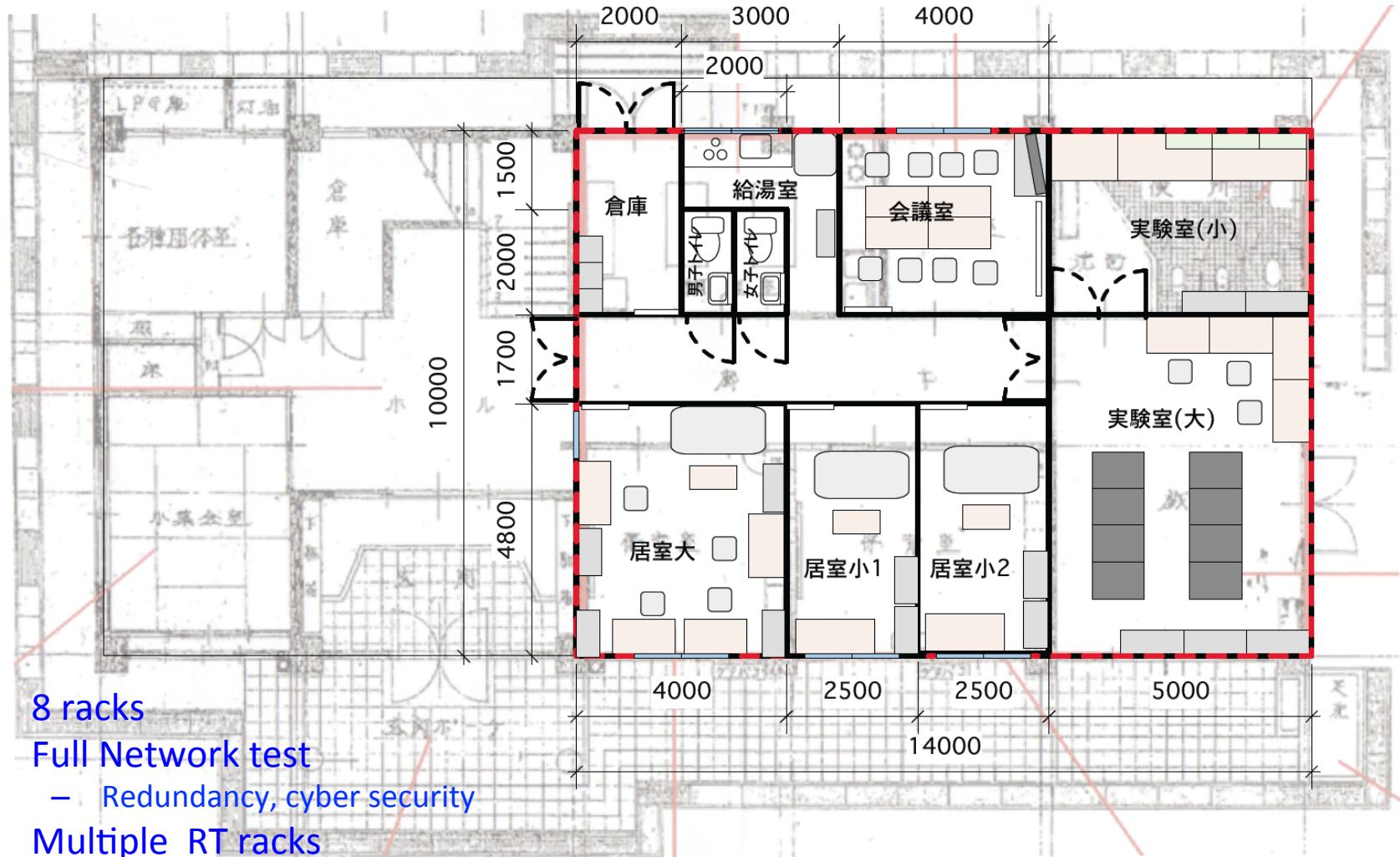
- Commissioning on site?
 - Simulated plant
- Generally, they start thinking after subsystem setup exists.
- Let's start thinking DAQ interface and control software right now!
 - Number of channels
 - Interface
 - Channel name
 - Control topology



2-4. Quality assurance: C. Small network test



2-4. Quality assurance: D. Full test at Kamioka





2-4. Quality assurance: Full system

All below items are being discussed and will be ordered as a full LCGT control system

- ADC ~100, DAC ~50, BO ~100
- AA 100 case, AI 50 case, BO 100 case
- Remote IO chassis ~30
- RT PC ~30
- Servers ~10
- Control WS ~10
- Security, redundancy
- Data storage (~500TB)
- Network switches
- Timing
- Full channel test
- 3km test



2-5. Installation scenario: Construction of full digital system

- Installation of whole system: just moving from Kamioka new facility into LCGT mine in the middle of FY2014
- Installation of RT racks for subsystem
 - Making a RT rack module:
 - RT PC, IO chassis, AAs, Al's, BO interfaces, power supply,
 - Add RT racks to full system (network boot)
 - When?
 - depends on the installation of subsystems.
- Commissioning
 - Cable
 - Wiring
 - Noise level, TF check
- Maintenances
 - Software update
 - Hardware upgrade (ex. LIGO: every 3 or 4 years)



2-6. Risk management

- Cyber security: P=1, S=2 -> R=2
 - Needs professional level network security system
- Huge number of channels: P=2, S=2 -> R=4
 - How do we check huge number of channels for analog and digital to avoid troubles?
 - Make a redundant system
- Commissioning on site: P=2, S=2 -> R=4
 - Simulated plant

The estimated probability P:

- 0 The probability is extremely low and will almost never occur.
- 1 The probability is not large and will probably not occur.
- 2 The probability is around 0.5.
- 3 The probability is large and will probably occur.

The degree of seriousness S:

- 0 It will not affect the successful completion of the project.
- 1 It will to some degree affect the successful completion of the project.
- 2 It will to some degree endanger the successful completion of the project.
- 3 It will result in the failure of the project.

If the degree of risk $R = P \times S$ is equal to or larger than 2, show backup plan.



Needs more manpower

- Activity for development: Miyakawa (whole) and Kamiizumi (circuits)
- Activity as users: Hayama (data pipeline), Michimura (R&D), Takahashi (VIS)
(Official members: Miyakawa, Aso, Izumi, Kamiizumi, Michimura, Miyoki, Ohishi, Saito)
- Needs more developers in the next 2 years for important development term
 - Development for Slow EPICS controller
 - Circuits design for subsystem's interface including whitening/dewhitening and variable gain amplifier
 - Simulated plant (for students?)
 - Computer hardware expert including network
 - Computer software expert
 - Commissioning people



3. bLCGT

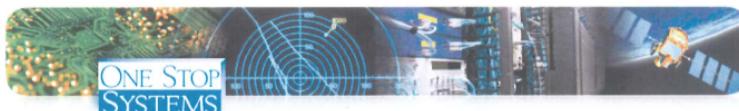
- Essentially no difference for digital subsystem between bLCGT and iLCGT because of budget limitation.
- We will install all RT computers, client WSs, network computers and networks(RFM, timing, DAQ, general) when iLCGT is installed.
- Channel number will be limited at the installation of iLCGT and it grows up during commissioning of iLCGT and bLCGT.
- Upgrade for hardware should be considered. Ex. LIGO is planning to replace PCs every 3-4 years. In any case, initial design can support bLCGT spec.



Appendix A. Design changes that have been made with the suggestions in the 1st external review

Development for Remote IO chassis

The committee has some concern regarding the installation location adjacent to the interferometer vacuum chambers. Such proximity has led both the LIGO and VIRGO projects to relocate their electronics racks to separate rooms. We suggest considering the installation of all electronics in a separate rooms, as recommended in our discussion of the tunnel design.



PCIe x4 Active Optic Cable

Fiber optic cable with PCIe x4 connectors.
OSS-PCIE-CBL-ACT-x4-10M
OSS-PCIE-CBL-ACT-x4-100M



- Available in 10m and 100m lengths
- PCI-SIG PCI Express Cable Specification Compliant
- Positive latching mechanism per the PCI-SIG specification

TECHNICAL SPECIFICATIONS

PCIe x4 Active Optic Cable

Cable Length	10m, 100m
Data Transfer Rates	PCIe Gen 1 – 10Gb/s PCIe Gen 2 – 20Gb/s PCIe Gen 3 – 32Gb/s
Gender	Male-Male
Temperature Range	-Case operating 0° to 70°C
Lock to Mating Part	Yes
Fiber Cable Diameter	3.0mm
Wire/Cable Type	Round

PCIe x4/x8 Gen 2 Expansion Board

PCIe x8 or x4 Gen 2 expansion link board installs in SHBe slot of a PCIe Gen 2 backplane, allowing either x8 or x4 cable inputs from upstream host system.

OSS-SHB-ELB-x4/x8-2.0



- Can connect PCIe x4 and x8 lanes
- Each puts out PCI Express 2.0 lanes to backplane
- Lanes are auto-configurable to backplane or can be user configured
- Lane active LEDs on slot cover
- Power acceptable LEDs on board

TECHNICAL SPECIFICATIONS

PCIe x4/x8 Expansion Link Board

Form Factor	PIGIG 1.3 SHB Express system slot compliant
Slot Type	System slot for the expansion chassis
Dimensions (H x L)	4.375 x 6.6 in (111 x 161 mm) 1 slot wide
Switch	PLX PEY632 32 lane switch
Upstream Interface	PCIe x4 over cable, PCIe x8 over cable
Downstream Interface	20 lanes of PCI Express can be auto-configured as: One x16 and one x4 PCIe link, Two x8 and one x4 PCIe links, or five x4 PCIe links
Front Panel Connectors	1 PCIe x4 cable connector, 1 PCIe x8 cable connector
Front Panel Indicators	1 green LED for x4, 1 green LED for x8
Internal Indicators	Power In-range Indicators for +2V, +3.3V & VTT (Red/Green), Power on indicator for +5V (Green), Bank of 5 board status indicators (Red)
Optional Features	Heat Sink: On-board fan header provided for optional heat sink fan
Temperature	0° to 50°C (32° to 122°F) default -20° to 70°C (-4° to 158°F) with optional fan heat sink
Storage Temperature	-40° to 85°C (-40° to 185°F)
Operating Humidity	10 to 90% non-condensing
Storage Humidity	5 to 95% non-condensing
Shock	3g acceleration peak (11ms pulse)
Vibration	5-17 Hz 0.5" double amplitude displacement; 7-2000Hz, 1.5g acceleration
Power Consumption	9W typical, 11.4W max, +12V @ 0.675A max, 3.3V @ 1.0A Max, 5V aux @ 2.5mA max
Agency Compliance	Designed to meet: FCC Class B, CE, RoHS

ONE STOP SYSTEMS

- No fan for calm environment
- Development and test with 6 prototypes in FY2011, FY2012
- IO chassis test for ADC/DAC and BO with existing aLIGO type timing system for short/long distance



Appendix B. Items that have been reduced in cost (if any)

None