



Status report from digital system subgroup

2011/8/4(Thu) LCGT f2f meeting

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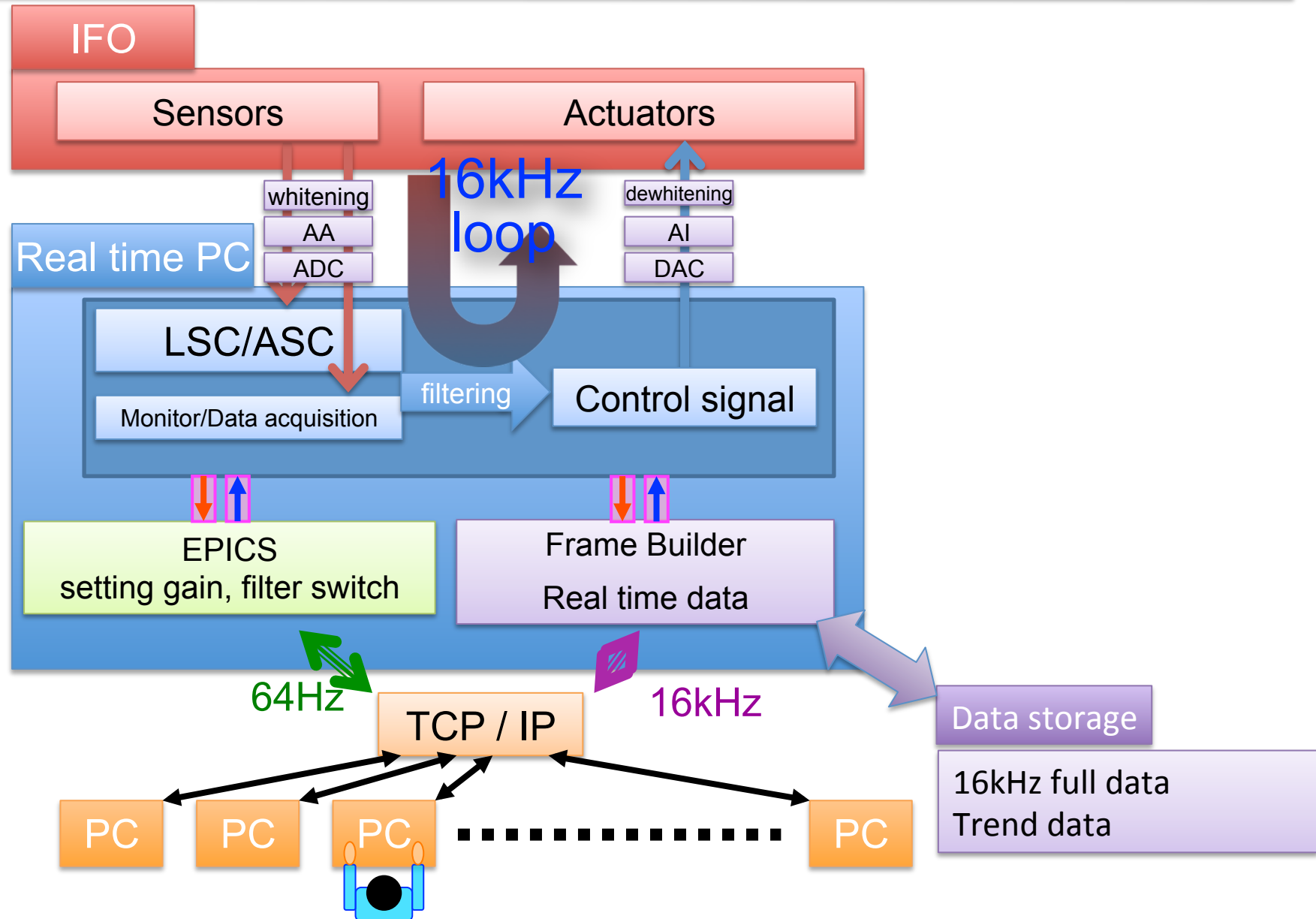


Summary of work from last f2f

- As of the last f2f meeting, visited to Caltech and constructed a stand alone system, and looked at a CDS test bench for aLIGO at LHO
1. Re-construction of **2-3 standalone systems** using Gentoo Linux distribution with RT patch based on vanilla Linux kernel and Ubuntu **workstation benches**
 - Currently we are working on making circuits for distribution
 2. Construction of a **small network test bench** consisting of 1 master PC and 2 slave RT PCs, connected by two types of **Reflective memory network** and **DAQ network** using open-mx technology
 3. **Timing system** using GPS synchronizing multiple PCs with 1PPS signal.



Concept of the digital system



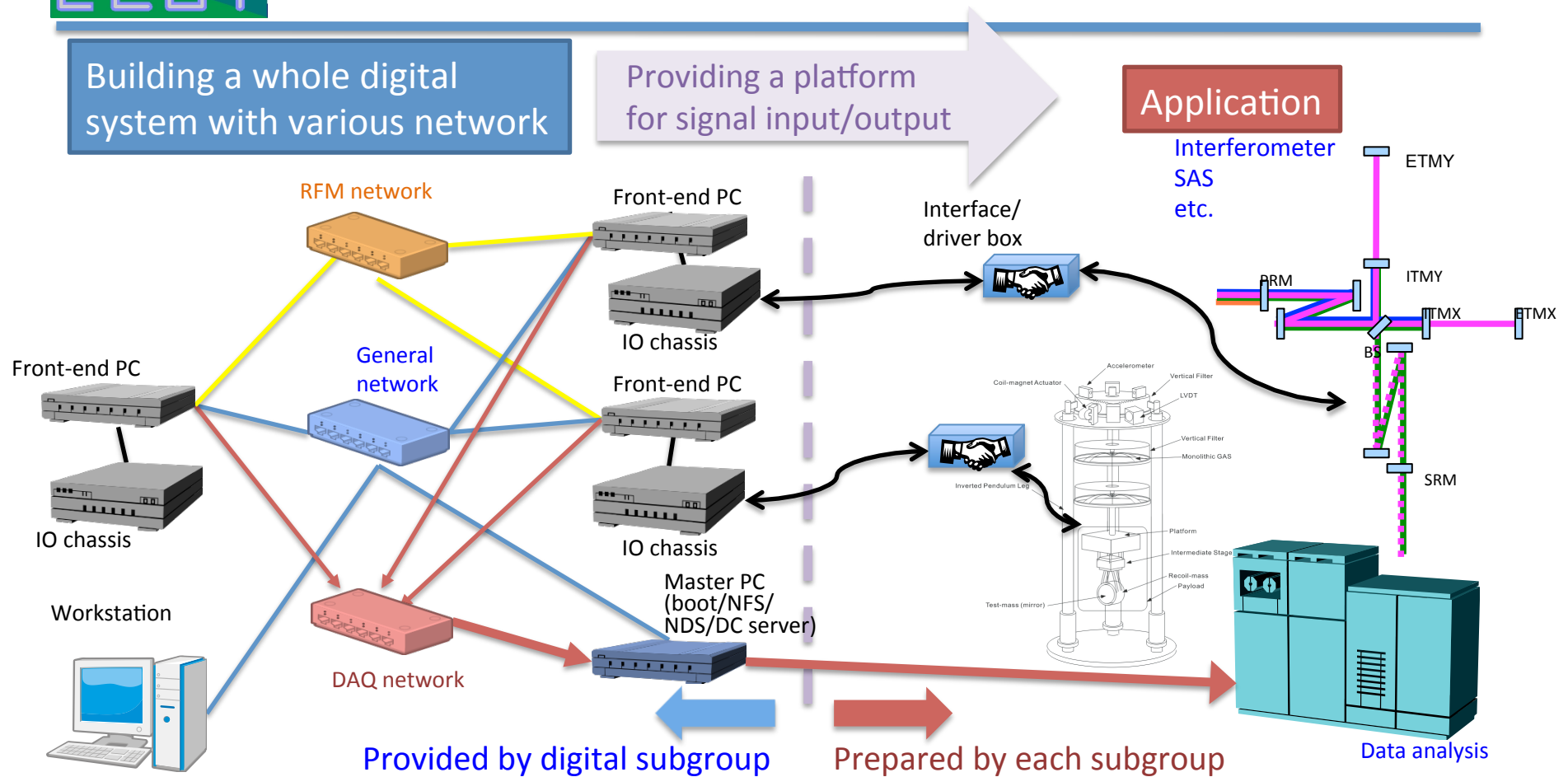


Digital system will be a critical technology for commissioning/noise hunting

- Provides a very flexible human interface for a very complicated DOFs of the interferometer.
- Good solution to treat huge numbers of signals in Large scale interferometer
- Provides many useful functions as sensing, filtering, Matrices, controls, monitoring, switching etc.
- Multiple people can work at a time



Overview of digital system



- Real Time Front-end PC
- Workstation, Diagnosis software
- ADC/DAC/BO in IO chassis, AA/AI
- DAQ/RFM/timing network

- Control, monitor, switch
- Auto lock, auto alignment
- Commissioning, noise hunting
- Diagnosis, tuning, calibration
- Operation, observation



~FY2010: Development of **prototype system** at/using CLIO

FY2011: Delivering **stand alone system** to subgroups

FY2012: Test operation system as **whole network** at Kamioka building

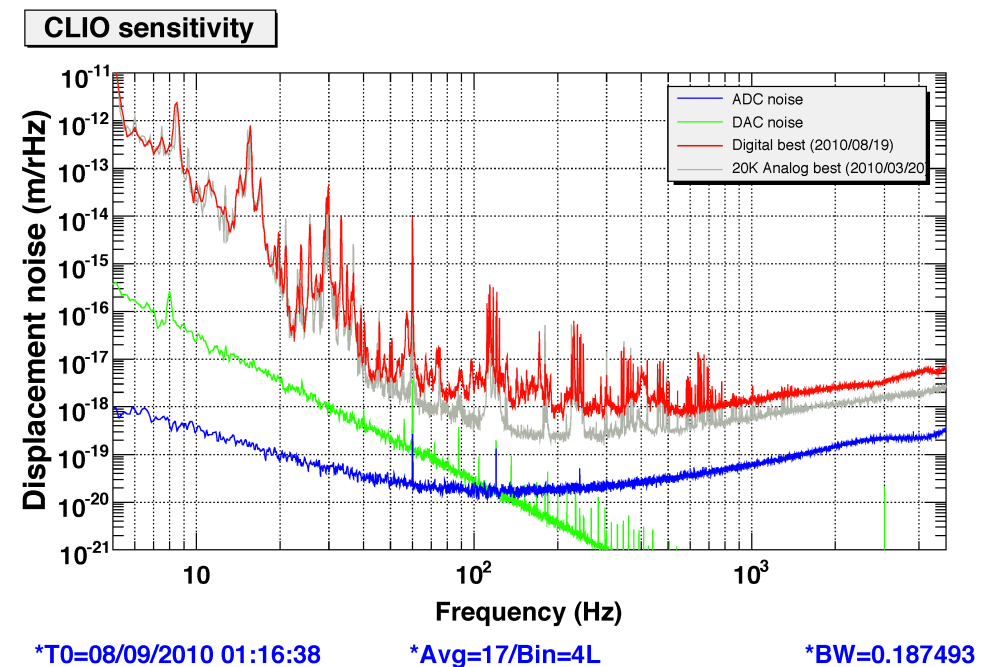
FY2013~: Installation of full digital system into mine

FY		2010				2011				2012				2013				2014				2015				2016			
Quarter		1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
Main Phase		Design				Tunnel								Vacuum				FPMI				RSE				Cryo			
Prototype test	CLIO operation	■	■	■	■																								
	Data analysys test							■	■	■	■	■																	
Standalone system for subsystems	Hard/software setup				■	■																							
	Circuit				■	■	■	■																					
	Delivery						■	■	■																				
Article test	Small network					■	■	■	■																				
	Large network sytem									■	■	■	■	■															
Full system installarion	LNS->full system													■	■														
	Software setup														■	■	■												
	Cuircircuits															■	■	■											
	Newtwork																■	■	■										
Upgrade	RSE																	■	■	■	■								
	Cryo																									■	■	■	■



Prototype 1: test in CLIO ~2010

- To establish the first test of aLIGO type digital system
 - Obtaining equipment in Japan like ADC/DAC/BO, IO chassis...
 - Related analog circuits like AA/AI, WF/DWF
- Lock acquisition
 - linearizing error signal
 - normalizing power
- Calibration process on DTT
 - sensitivity monitor
- Noise performance
 - Switching WF/DWF by BO
- Auto alignment
- Application for other R&D experiment



1 day Engineering run is planned using CLIO in this fall
for development online analysis software



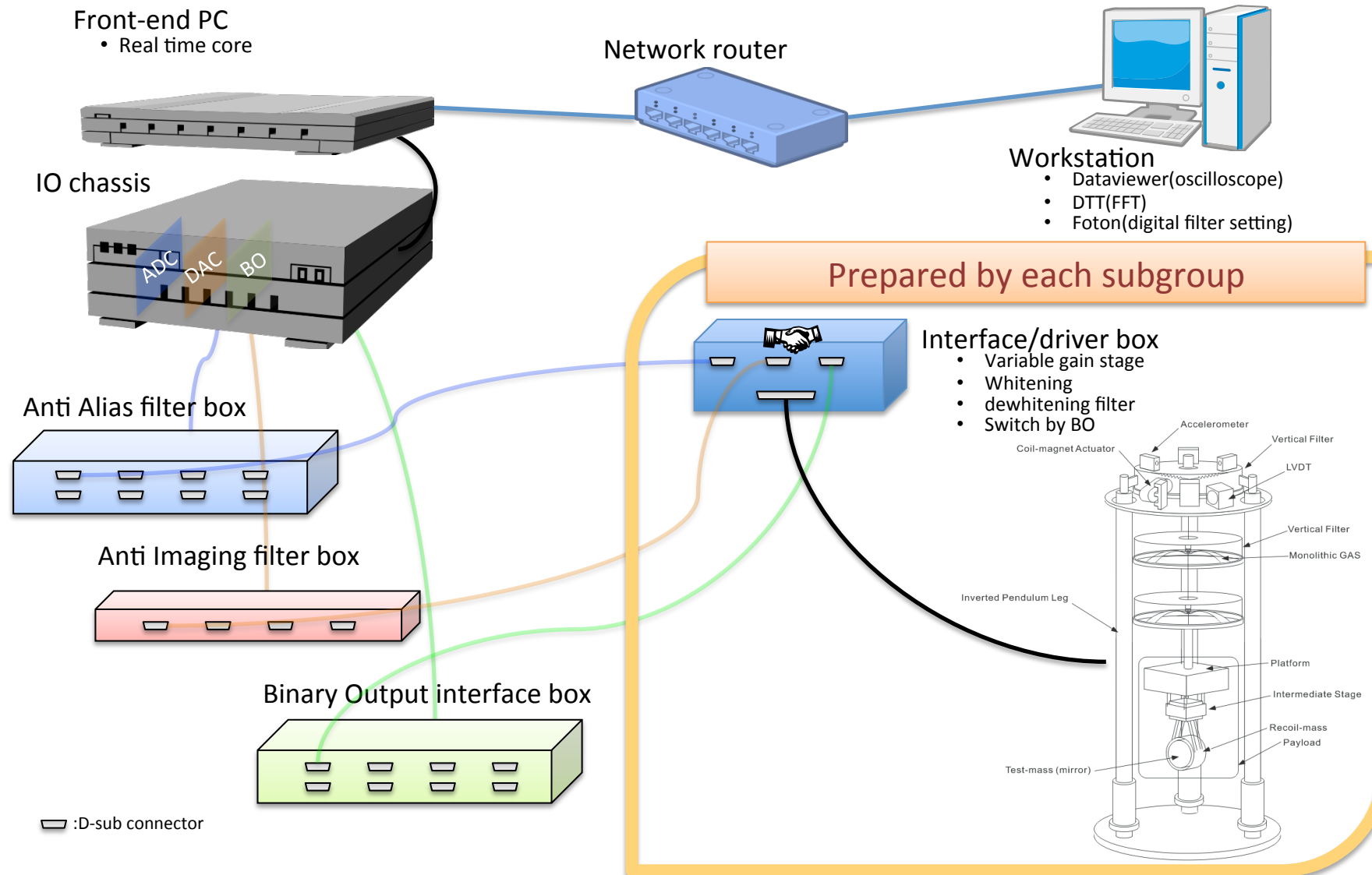
Prototype 2: Standalone system for subsystems

5 sets of stand alone digital system will be delivered to subgroups in FY2011

1. Real time control computer as front-end
 2. Client workstation PC with software setup
 3. PCIe I/O chassis for ADC/DAC/BO modules
 4. Timing slave board
 5. ADC, DAC, Binary Output
 6. Anti Alias/Anti imaging filters
- good chance for subgroups to use a digital system before the commissioning of LCGT
 - Network diagram: JGW-D1100404
 - Additional distribution:
 - Tsubono group (HDD only)
 - NAO for data analysis



Connecting subsystems into digital system





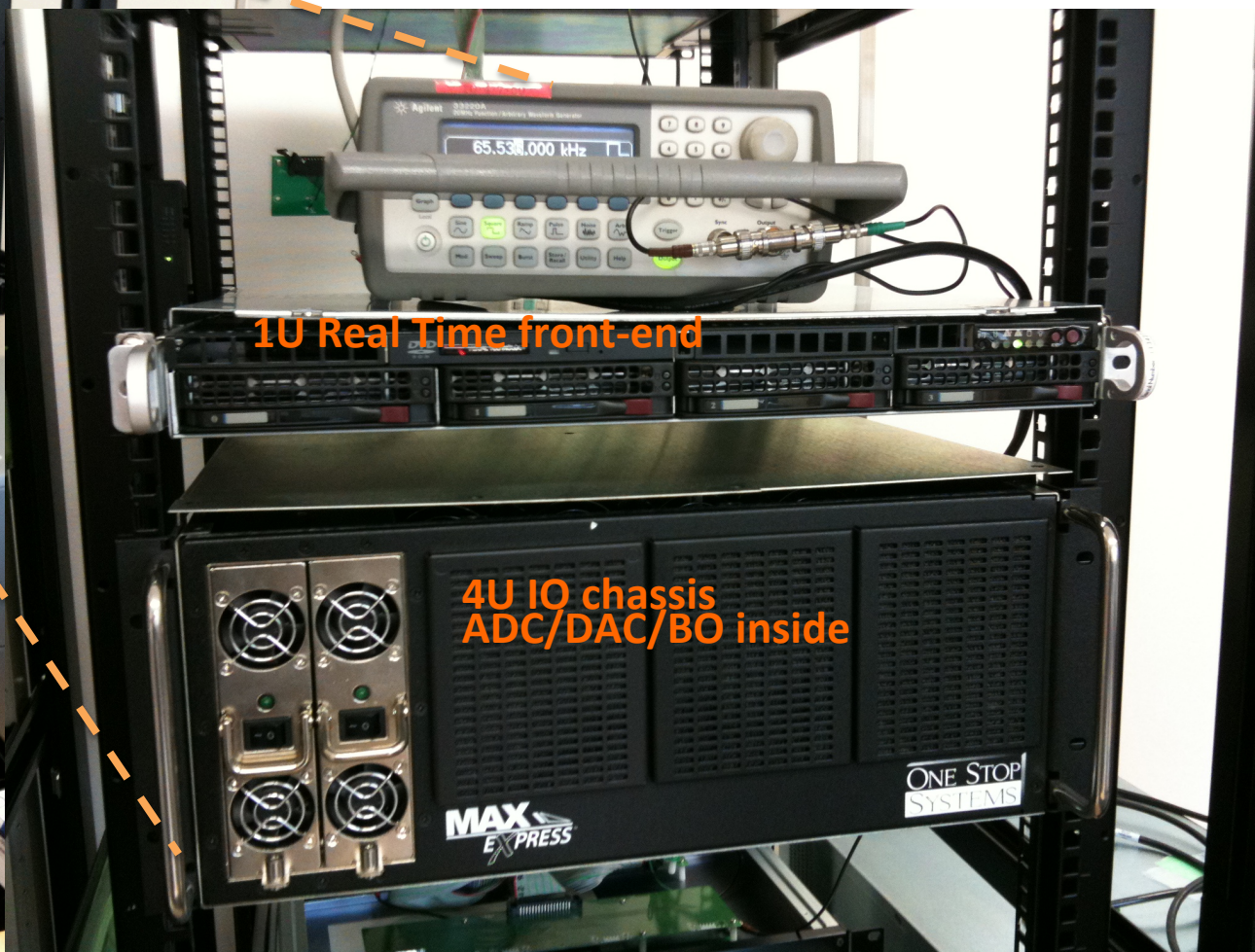
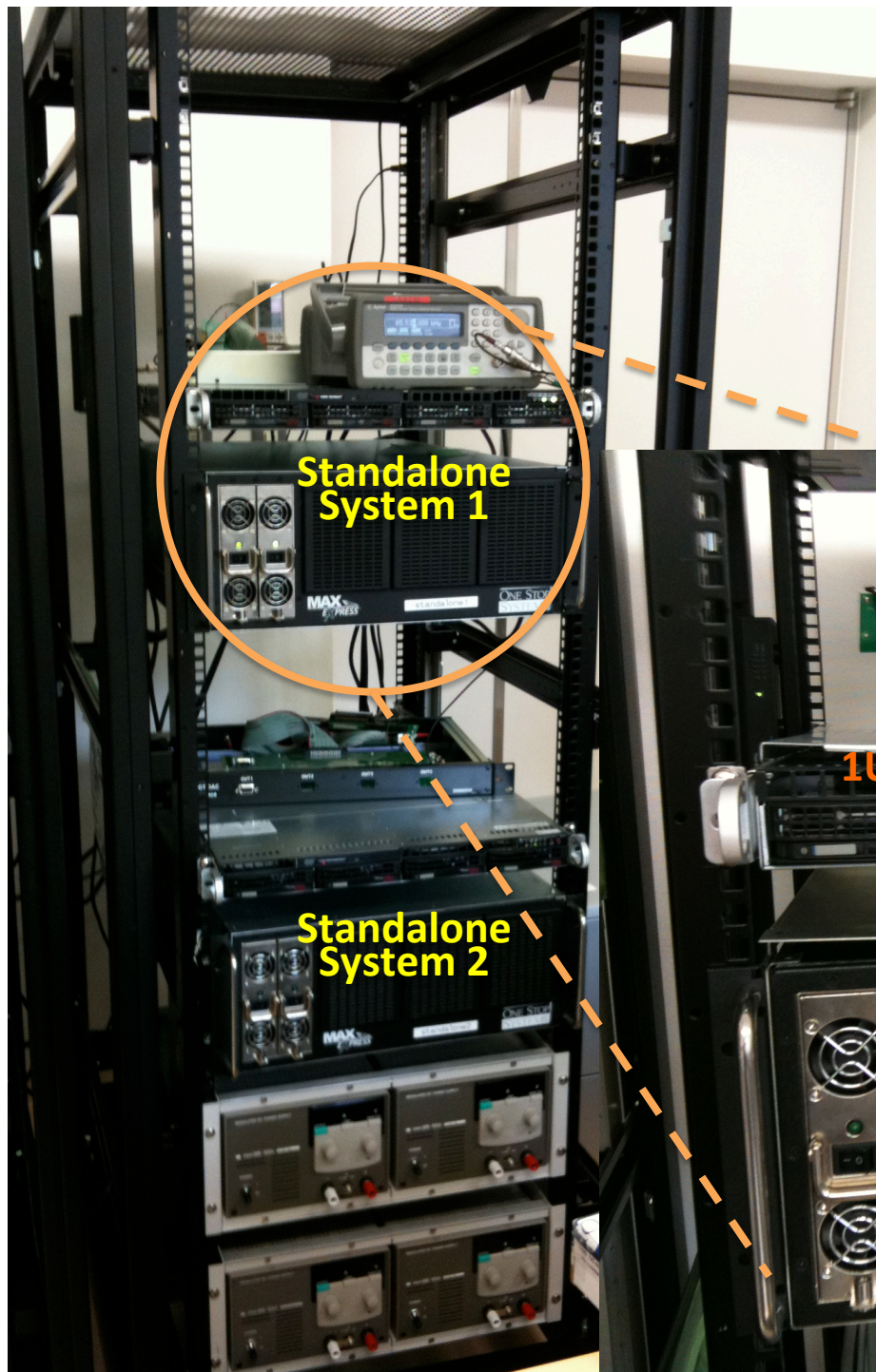
Troubles in Standalone system

1. DAC trouble

- Could not produce output signal
- Fixed by making multiple models in one PC which have a relationship of master and slave

2. Unstable connection with IO chassis using HIB

- GEN1 (HIB2) or GEN2 (HIB25)?
 - LIGO fixed using GEN1 card, but not for ours
- Cable length?
- Not fixed yet



Client system

MEDM

DTT (FFT)

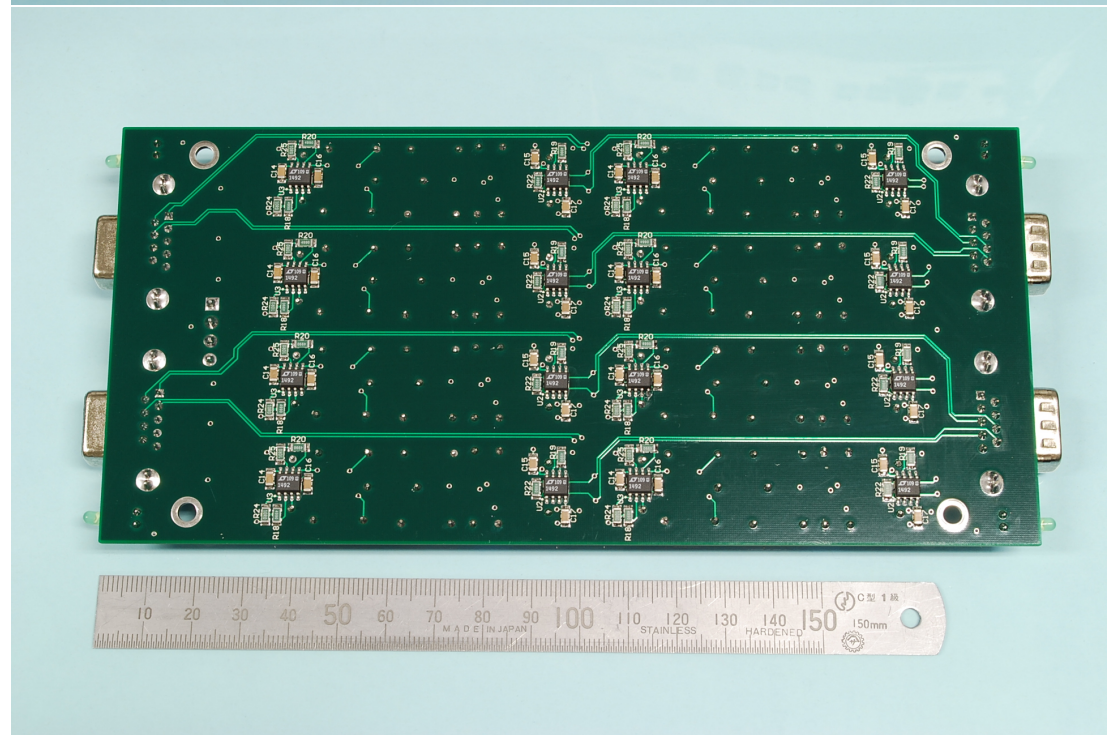
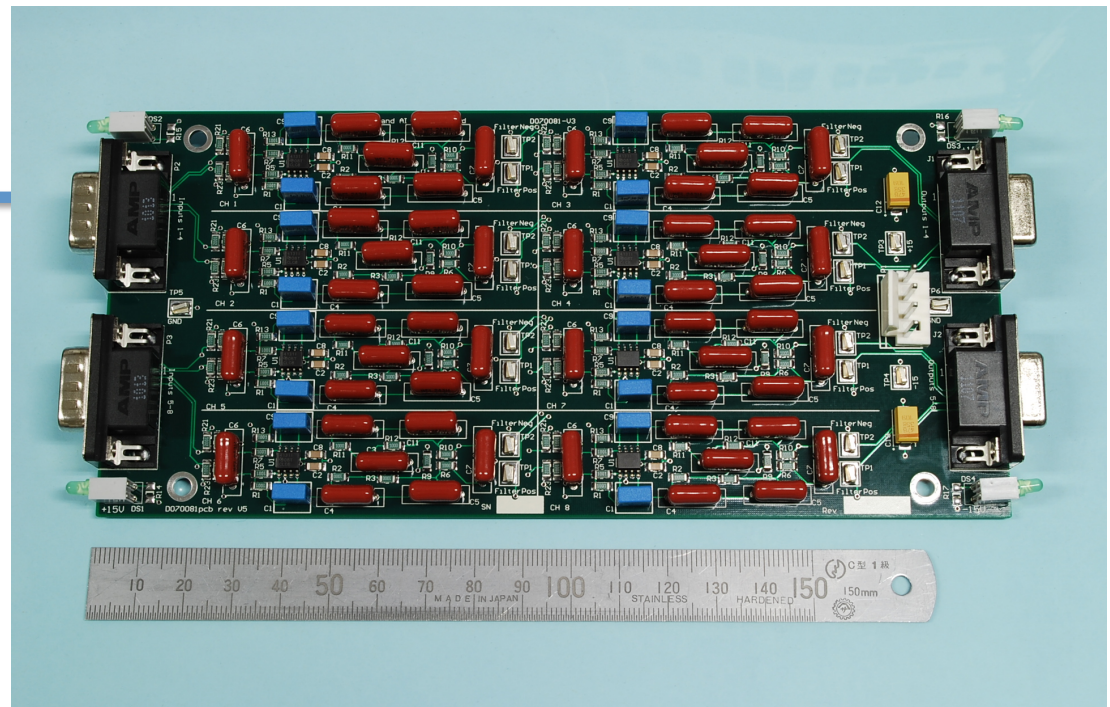
Foton
(filter composition)

Dataviewer
(oscilloscope)

Striptool
(long term monitor)

LCGT AA/AI board

- Manufactured by P-ban through Analog circuit group, thanks Moriwaki-san!
- 10 LIGO designed AA/AI boards ordered
 - 6 layers circuit board
 - auto mounted
 - Soldered
- Needs:
 - power supply board
 - Interface boards
 - 1U box





Standalone system to network system

- Standalone digital system is not so difficult:
 - No time loss in local memory
 - GW data locally stored
 - No timing required
- Real time control using **multiple PCs will be much more difficult** for the **speed of network** with bandwidth and delay
 1. **Control signal**: small amount of data, but only minimum delay acceptable for real time control
 - > Reflective memory
 2. **GW data**: not so strict for speed as control signal but only tiny delay acceptable for time stamp, and very wide bandwidth for Huge amount from many RT PCs
 - > Myrinet or Open Myrinet
 3. **Synchronization** for all ADC/DAC and all PCs
 - > Master/Slave style timing system



First Article test

1. Small network test in FY2011

- Network among 1 master and 2 slaves
- GE RFM, Dolphin RFM, DAQ, timing network

2. Full network test in FY2012

- ~8 network PCs
 - 1 boot/nfs server
 - 1 data concentrator server
 - 2 nds servers for redundancy
 - 2 frame writers for redundancy
 - 2 gateways for redundancy
- 2 data storage devices for redundancy
- ~7 RT front-end PCs
- ~5 Workstations
- Multiple RFM/Dolphin/DAQ/general network hubs
- Redundancy test



Small network test at Kashiwa campus

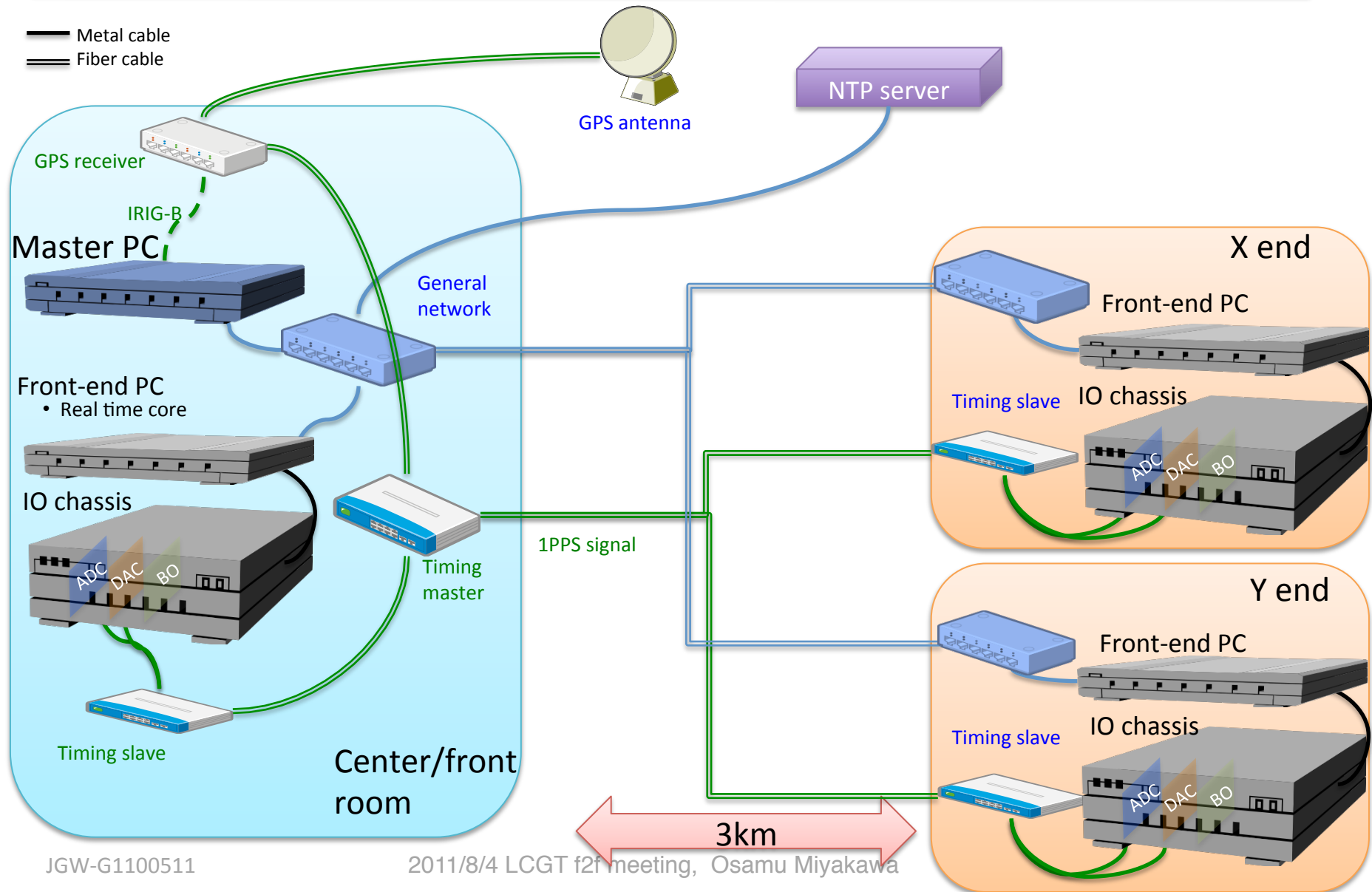
- Man power: Joseph Betswiezer (Caltech post-doc, 40m's main CDSer) and Osamu Miyakawa
 - Lecture for students of Tsubono group for standalone system

What we did are:

1. 1 master PC as a boot server, and PXE booted 2 slave PCs
2. Timing system
 - GPS antenna and receiver
 - LIGO Master/slave timing system
 - 1PPS synchronization into each ADC card on 2 slaves
 - IRIG-B signal is necessary for master synchronization in the future
3. GE Reflective memory hub using fiber cable connection between 2 slaves
4. Dolphin reflective memory hub using metal cable connection between 2 slaves
5. DAQ network with open-mx protocol
 - Myrinet card is necessary for data concentrator in future

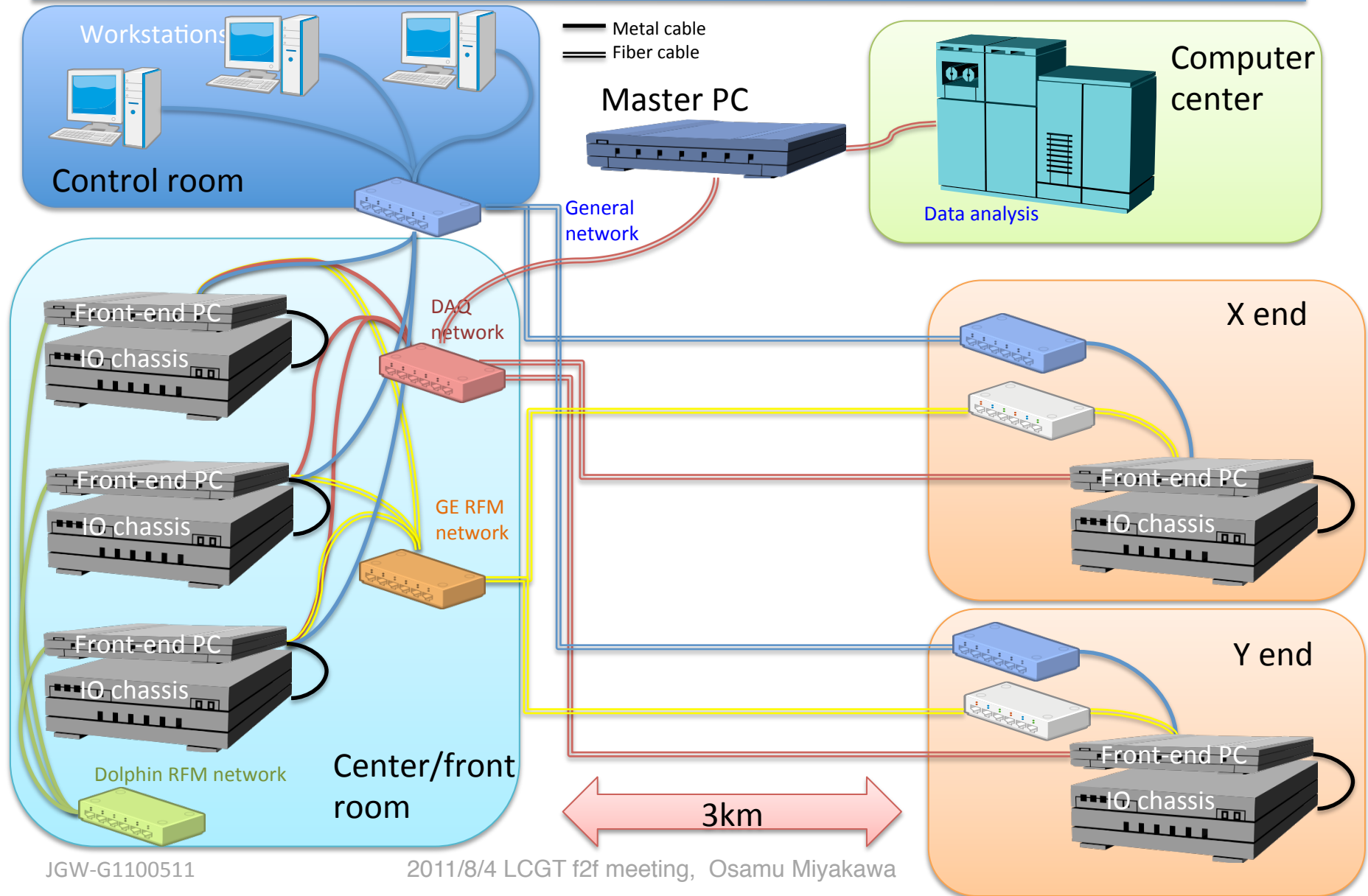


Timing Network



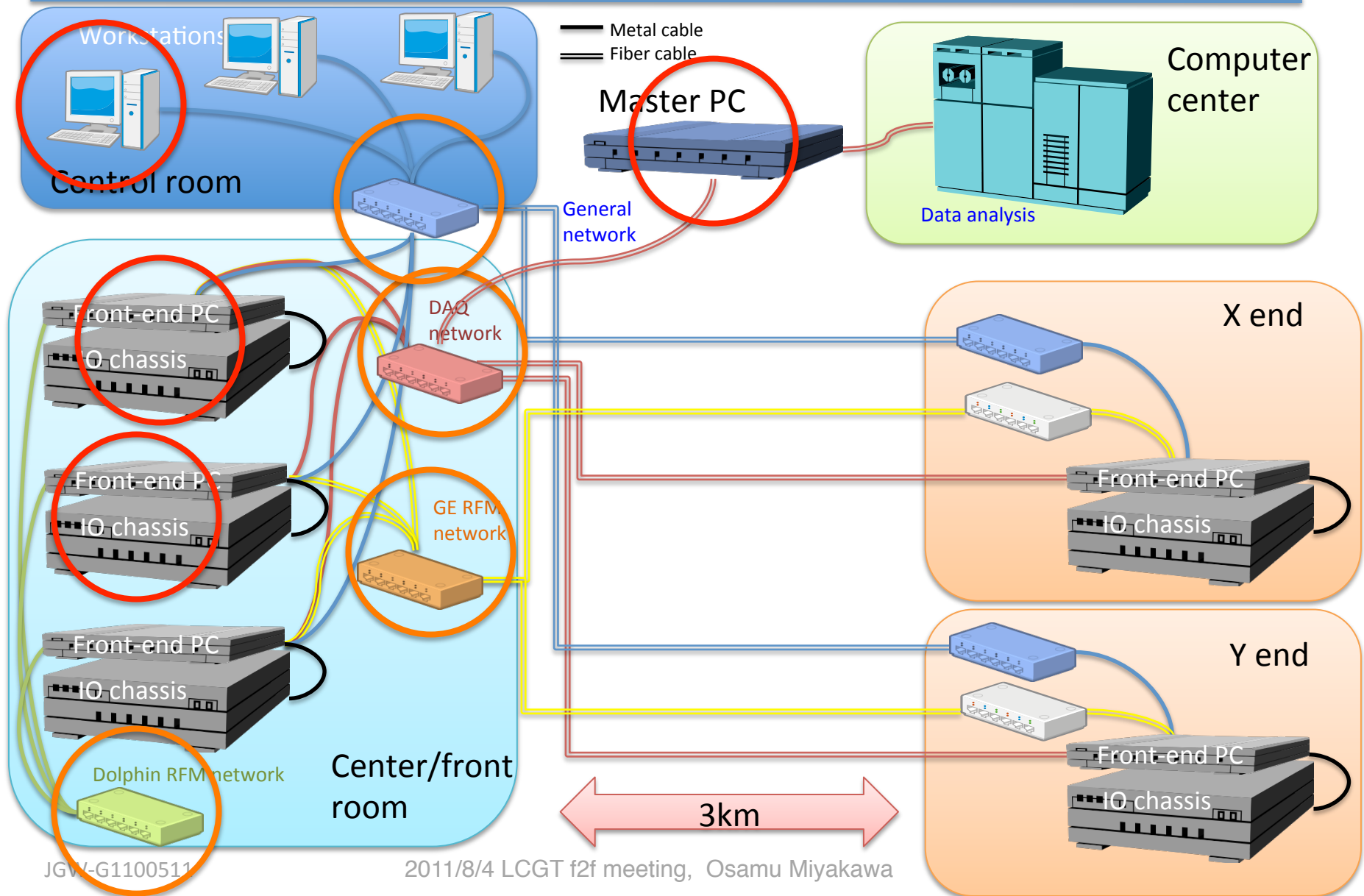


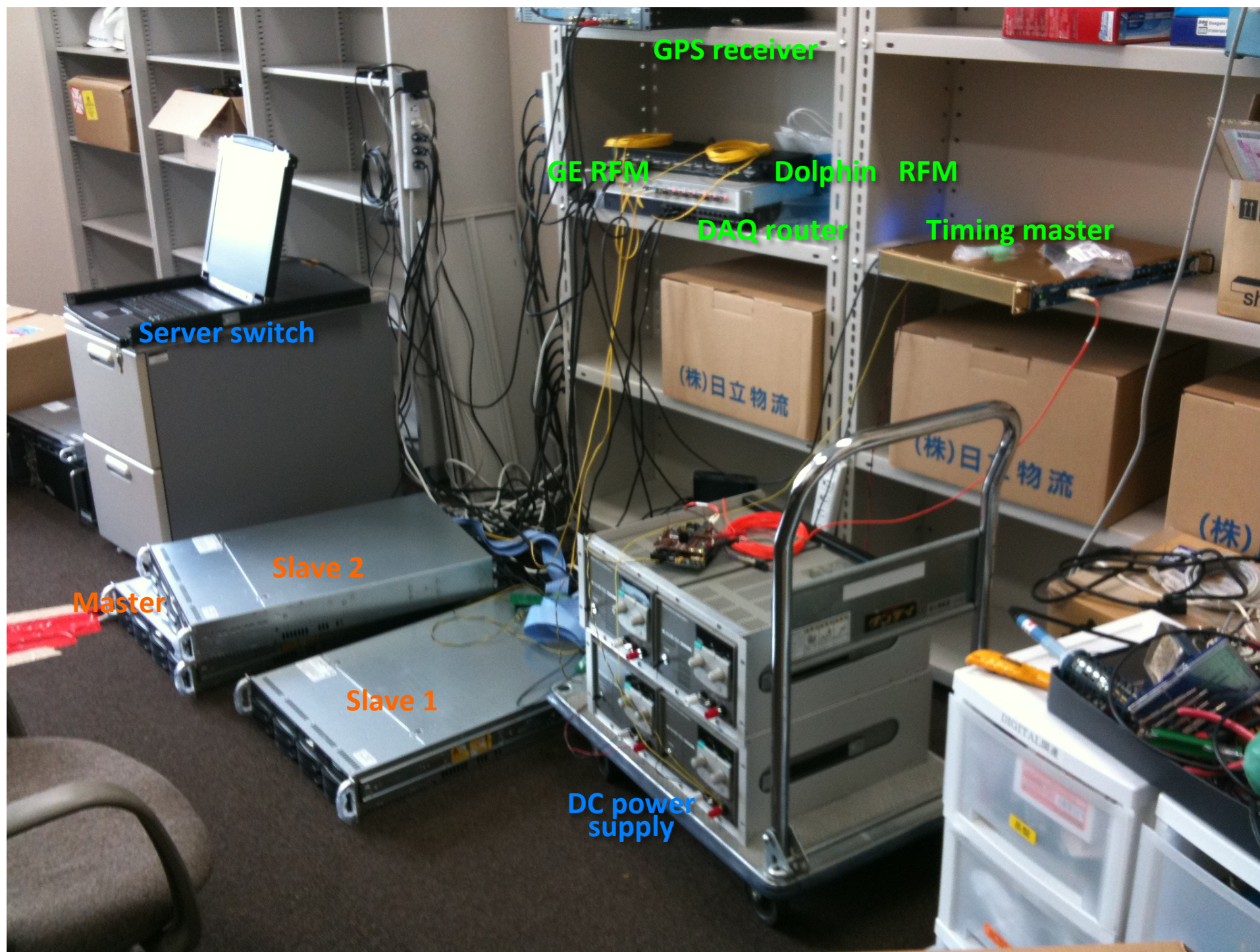
Network design





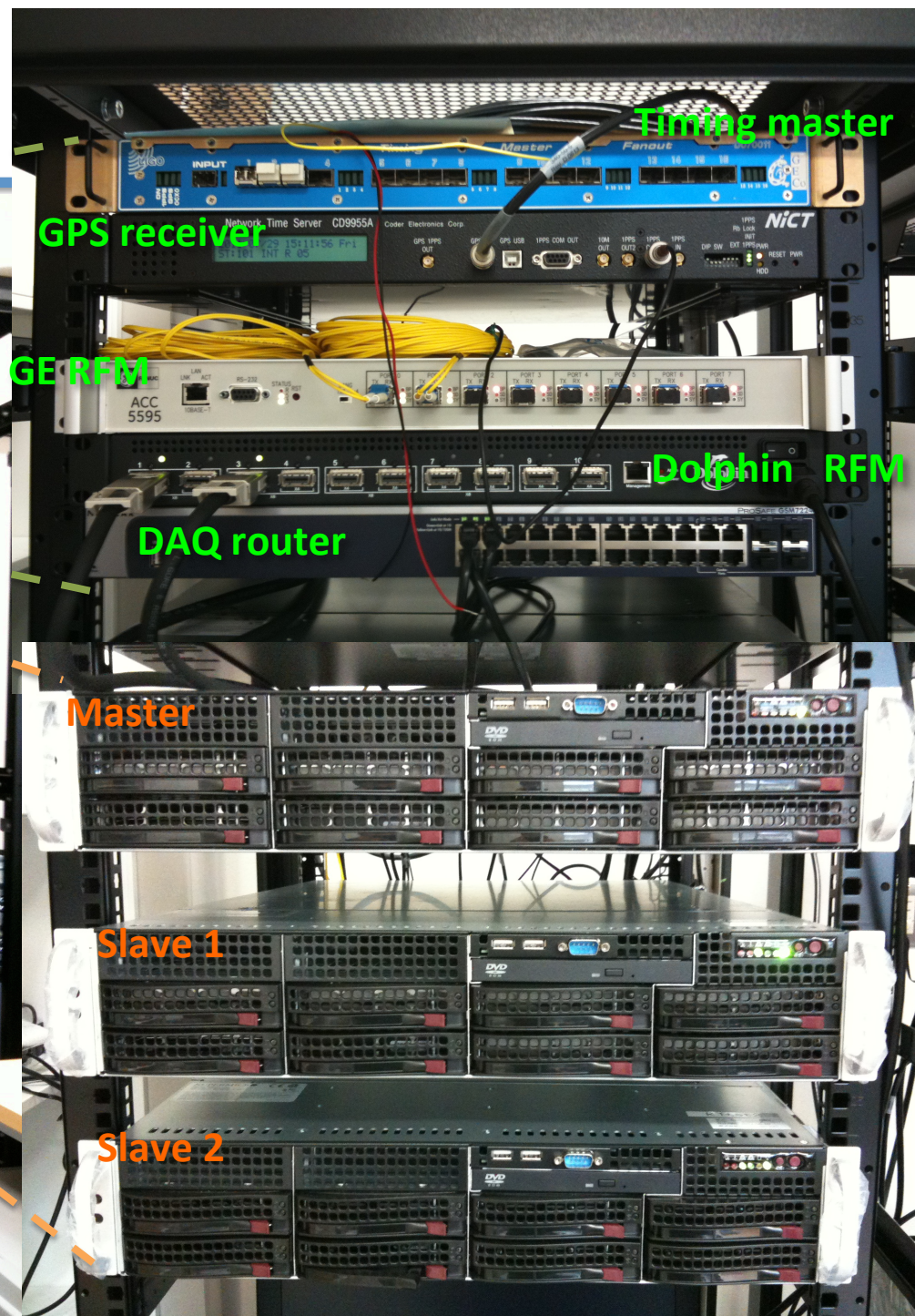
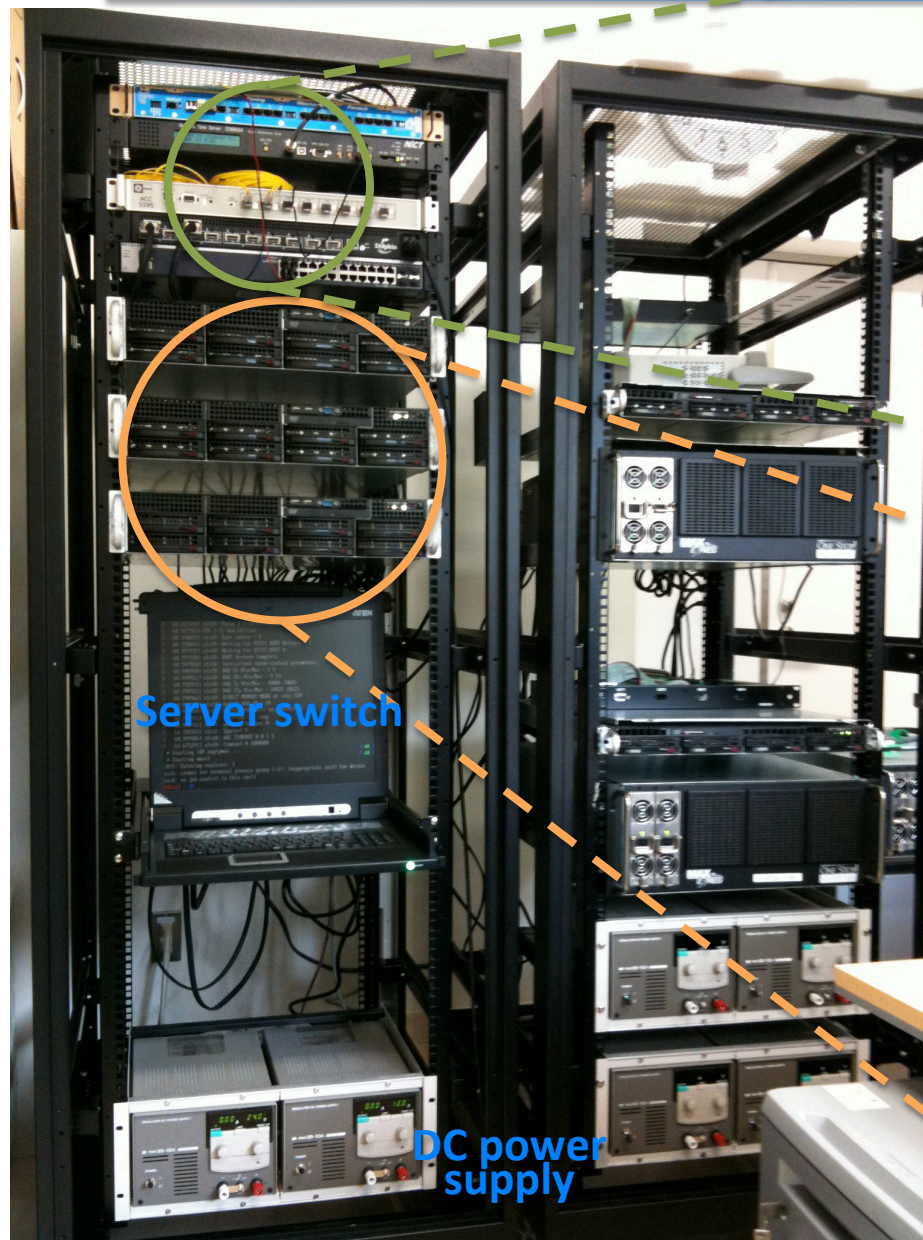
Network design







Re-construction at Kamioka





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Risks

- Cyber security
 - Needs professional level network security system
- Redundancy
- Huge number of channels
 - How do we check huge number of channels for analog and digital to avoid troubles after installed
- It is important to understand whole digital system from inside and it is also important to keep communicating with LIGO CDS group.