External review for digital system

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Digital system subgroup member

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1. Design for bLCGT

1-1. Definition of Subsystem

Digital system (DGS) subgroup provides a flexible human interface for a km large scale interferometer. This system has the functions which digitalize analog sensing signals extracted from the interferometer and subsystems, produce signals in the computer for controls, monitors and data acquisitions, and re-produce analog signals to actuate the interferometer.

This subsystem has following items.

I. Development of real-time (RT) control computer
   (a) Signal input/output using ADC/DAC modules
   (b) Binary switch using BO modules
   (c) Real-time software for monitor/diagnosis
   (d) Real-time communication network interface
II. Development of client workstations (RT system monitor) for monitor/diagnosis
III. Network design and development for following data transfer
   (a) Real time control
   (b) Timing
   (c) Data acquisition (DAQ)
   (d) General network
IV. Producing frame data for data storage/analysis

Note that we ask each subgroup to develop the application software like real-time interferometer control model, data analysis software using frame data and so on. We offer a typical model for application software and instructions/lectures for how to use the digital system.

1-2. Requirements

Global requirements for this subsystem should come from Detector Configuration (DET) subgroup or Main Interferometer (MIF) subgroup and other related subgroups. Items of the global requirements will be something like that;

I. Observation bandwidth
II. Dynamic range
III. Control bandwidth
IV. Number of input channels
V. Number of output channels

Since the global requirements have not been shown for our digital system subgroup, we assume appropriate minimum global requirements here.

Observation bandwidth >5kHz
Dynamic range >120dB
Control bandwidth >200Hz
Number of channels >1024
Number of output channels >256

Required dynamic range is determined by the amplitude and noise of error signals of interferometer during GW observation, or by how much dynamic range the lock acquisition needs. Reason for this 120dB is explained in Appendix A.

To satisfy this requirement, we define our internal requirements in Table 1. We selected 16bit ADC/DAC for the required dynamic range. From this table, the dynamic range of ADC will be >15V/3uV=134dB and the dynamic range of ADC will be >10Vpp/3uV=130dB.

Item	**Requirements**	**Comment**
Sampling rate	>=16384Hz	65536Hz at ADC, then decimated to 16384Hz
ADC bit resolution	>=16bit	
Dynamic range of input	>=+/-15V	Differential input
Dynamic range of output	>=+/-10V	Differential output
ADC noise	<3uV/rHz	Effectively reduced by whitening filter

DAC noise	<3uV/rHz	Effectively reduced by dewhitening filter
time delay	<100usec	For >200Hz UGF
Input channel numbers	>2048ch	(16kHz:>128ch, 2kzHz:>512ch, 64Hz>1024ch)
Output channel numbers	>512ch	For mirrors, seismic attenuators, PZTs etc.
Stored channel numbers	16kHz:>64ch, 2kzHz:>512ch, 64Hz>1024ch, 16Hz>10000ch	~300TB/year

Table 1. Requirements for digital subsystem

1-3. Interface

1-3-1. Interface for signals

Our main interface to other subgroups is for the signal input/output and switch. These interfaces are defined as follows;

Signal input

- ADC 32ch/card, differential (64ch for single input)
- Sampling rate: 16384Hz
- Maximum input range: +/-20V
- Noise: 2uV/rHz
- Input filter: Anti alias filter
- Connector: D-sub 9pin* (for differential 4ch)

Signal output

- DAC 16ch/card (32ch for single output)
- Maximum output range: +/-10V
- Noise: 1.5uV/rHz
- Output filter: Anti imaging filter
- Connector: D-sub 9pin* (for differential 4ch)

Switch

- Binary output (BO) 32ch/card
- Output voltage: 0 or +5V

- Connector: D-sub 9pin* (for differential 4ch)
  (Ex. Variable gain amp for 16 steps/1 D-sub connector)

Note that D-sub 37pin may be supported for many channel transfer.

1-3-2. Frame data

Digital system subgroup is responsible for data acquisition and data formatting. All LCGT data will be formatted as the same as world standard GW data (like LIGO, VIRGO) through Frame Builder (FB). The FB is a part of digital system and produced data will be stored through DAQ network into raw data archive which is 100TB class RAID data storage located at the front room. This raw data archive is a temporary data storage that can be used for commissioning or pre-data analysis and so on at the local site. Stored data should exist at the local site for longer than 1 month at least. Data over beyond 100TB will be sent to another huge data storage, which will be prepared by data analysis subgroup and located in Kamioka-building or Kashiwa GW computer center (to be determined).

1-4. Preliminary Design

1-4-1. Hardware

Real-time Core (RTC) runs on computers with the following minimum configuration:

1) Dual x86 processors, with four CPU cores each.
2) Processor clock speed of 3GHz.
3) Eight (8) Gigabyte of memory.
4) Two Gigabit Ethernet interfaces.
5) One, or more, real-time network interfaces
   a. Reflected Memory (RFM)
   b. PCI Express (PCIe) network interface
6) A PCIe interface to the PCIe expansion chassis with a maximum of 14 PCIe cards installed.

1-4-2. Software

The software is divided into the following functional groups;

I. RTC Software:

(a) Real-time Sequencer (RTS): That software which performs the functions of scheduling and I/O interfaces for all real-time applications.

(b) DAQ: That software which performs the function of real-time data acquisition and data formatting.

II. Real-time Common Library: A standard real-time code library for use in all real-time user applications.

III. Real-time Support Software: The software necessary to communicate between the RTC and operational support and DAQ software via Ethernet connections. This includes:

(a) EPICS interface software

(b) Arbitrary wave form generator (AWG) / Test point manager (TPM)

(c) DAQ Network Interface

IV. Real-time System Monitor: Software to run on a designated real-time computer designed to monitor the overall status of all real-time systems and networks.

1-4-3. Related analog circuits

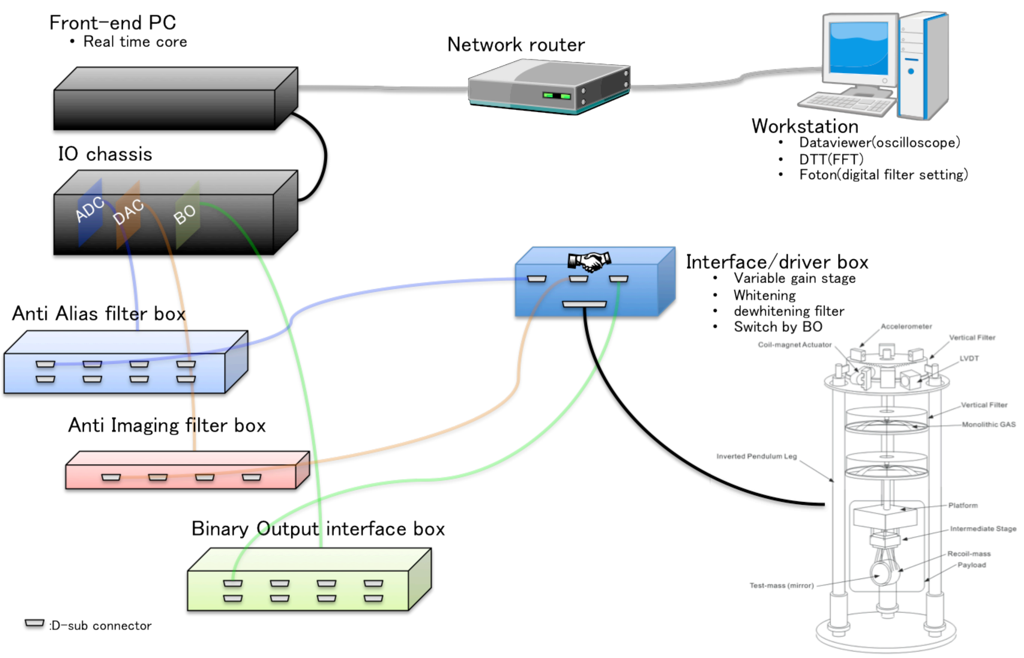

Figure 1. Typical connection between digital system and subsystems

An anti alias (AA) filter is required for ADC input, and an anti imaging (AI) filter is required for DAC output. Typical signal stream will be like following order;

I. Analog signal -> satellite box (including variable gain amplifier (VGA), whitening filter (WF)) -> long metal cable (~10m) -> driver box ->
II. AA filter -> ADC-> Computer -> DAC -> AI filter ->
III. Driver box -> long metal cable (~10m) -> satellite box (including dewhitening filter (DWF)) -> actuation signal

and the connection between digital system and subsystems is shown in Fig. 1. Digital system subgroup is responsible for II of this stream, i.e. analog AA filter and AI filter are provided by digital system subgroup, and other driver boxes and satellite boxes etc. should be manufactured by each subgroup. Typical circuit diagram will be offered from DGS subgroup.

AA and AI filter have the same frequency response that has a steep low-pass filter at the half of raw sampling frequency. In this system frequency of the low-pass filter will be set to 32768Hz.

Typical whitening/dewhitening filter has zero-pole/pole-zero for 15Hz and 150Hz or near around these frequencies. These frequencies will be tuned for what each subsystem needs. VGA should be also implemented upstream whitening filter with several gain steps which will be controlled by BO signals. For example, 4bit (of 32bit of one BO module) can have 16 steps, so one BO card can control 4 VGA in this case.

1-4-4. Rack design and location

All RT control computers, circuits, network equipment are mounted into 19 inch rack. Total 12-20 (depending on the number of channels) racks for digital system will be located inside LCGT (Fig. 2). Racks are categorized as following areas;

I. Front room (blue): length (1), WFS (1), auxiliary (1), network (1)
II. Laser room (red): Laser (1)
III. Center room (orange): Input optics(1-2), suspensions(1-3)
IV. Main suspensions (green): ITMX (1-2), ITMY (1-2), ETMX (1-2), ETMY (1-2)

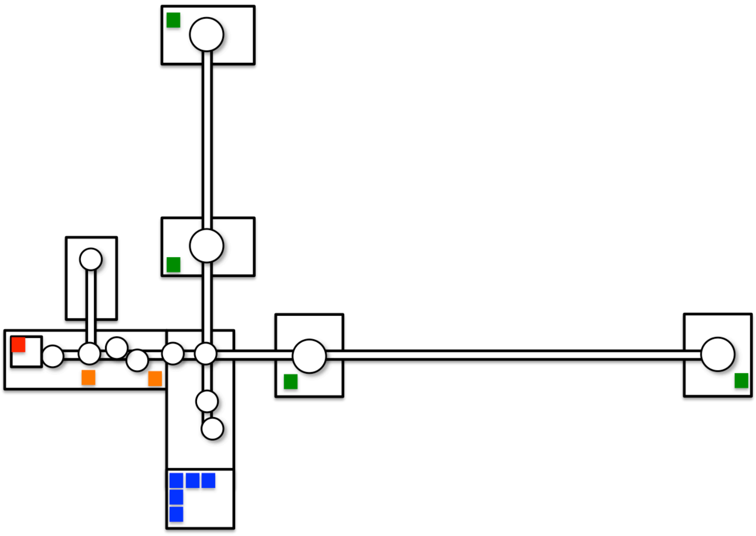

Figure 2. Location of racks for digital system.

1-4-5. Network design

We recognize that the importance and difficulties of a complicated huge network system with many RTS computers. The most important thing is how to connect the RTS computers for enough fast data transfer rates without any lose of lock for real-time control. We list up what kinds of networks are needed for LCGT here, and the simple schematic of whole network design is shown in Fig. 3.

I. Real-time control network: connection during RT computers for control
  (a) Reflective memory network (RFM)
    Hub: GE Fanuc 5595
    Cable: single mode fiber, <10km
  (b) PCIe network (Dolphin network)
    Hub: Dolphin DXS410
    Cable: metal or fiber, x10 faster than GE RFM, <100m

II. DAQ network: data collection stream from all RT control computers to raw data storage
  Router: NETGEAR 7224/7352, Fujitsu XG2600 or similar, through OpenMX

(10Gb network using open Mirynet protocol)

Cable: metal (CAT6 or 7) for PC-router, fiber for router-router

III. Timing network: timing distribution system (TDS) of absolute time for all RT control computers and 1PPS signal for ADC/DAC

GPS, frequency distributer, Master/Fanout/Slave aLIGO timing system,

IV. General network: PXE network boot for RT control computers, client workstations for control/monitor/diagnosis in control room, security and authentication, NAT, NTP, NFS, ilog, wiki etc.

Router: NETGEAR 7224/7248 or similar

Cable: metal (CAT5e or 6) for PC-router, fiber for router-router

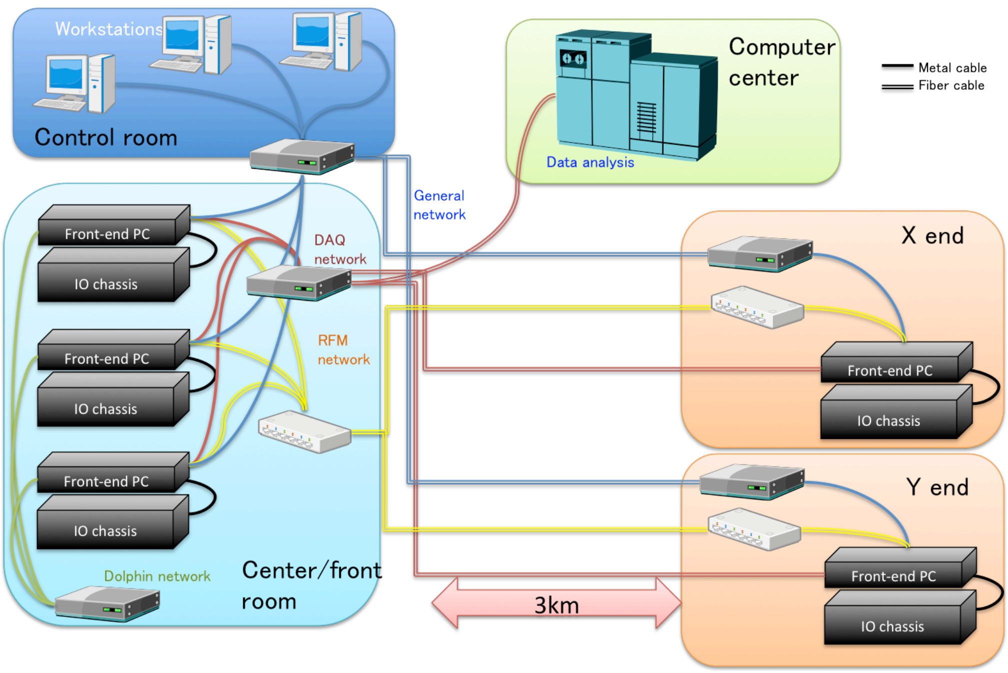

Figure 3. Conceptual connection diagram for whole LCGT network

1-4-6. Input/output channel list

a. ADC (total ~2048ch = 64cards or more)

Part	Channel point	Channel number	Description
Laser		10	
FSS	Power, REFL(DC, error), Trans	10	

ISS	Power, REFL(DC, error), Trans	10	
MZ	Power, REFL(DC, error), Trans	10	
PMC	Power, REFL(DC, error), Trans	10	
MC	Power, REFL(DC, error), Trans	10	
	WFS	12 (4quad x RF I&Q, DC) x2~30	
OMC	Power, REFL(DC, error), Trans	10	
	WFS	4x2~10	
LSC	AS, ASDDM(2), REFL, REFLDDM(2), POX, POXDDM(2), POY, POB, SPOB, DC	12 x 3 (RF I&Q, DC) + 1 ~ 50	
ASC	AS, REFL, POX	12 (4quad xRF I&Q, DC) x3 x2WFS ~ 100	
Oplev	14sus	4quad x14 ~64	
QPD	LPOS, LANG, IPPOS, IPANG, TRX, TRY	4quad x6 = 32	
SUS	64ch(2ADCa)*14sus	896	~100Hz
Vacuum		50	
Cryostat		400	~16Hz
PEM		100	

b. DAC (total ~512ch = 32cards or more)

Part	**Channel point**	**Channel number**	**Description**
PZT	Alignment for PMC, MZ, FSS, ISS, IMC	5x2 (pit, yaw) x 2 = 10	
WFS	Alignment to PD at REFL, AS	2 (pit, yaw) x 2PD x 2port = 8	
SUS	32(2DACs)*14	448	
Offset on analog servo	PMC, MZ, FSS, ISS, IMC, CARM	10	

c. BO (total ~2048bit = 64 cards or more)

Part	**Channel point**	**Bit number**	**Description**
Laser	Modulation index	2x4bit=8	
Gain slider	PMC, MZ, FSS, ISS, IMC, CARM etc.	10x4bit=40	
Servo on/off	PMC, MZ, FSS, ISS, IMC, CARM	10x1bit=10	

	etc.		
LSC whitening + switch	AS, ASDDM (2), REFL, REFLDDM (2), POX, POXDDM (2), POY, POB, SPOB, DC	12 x 3 (RF I&Q, DC) + 1 x 5bit ~ 200	
ASC whitening + switch	AS, REFL, POX	12 (4quad x RF I&Q, DC) x 3 x 2WFS x 5bit ~ 500	
Oplev whitening + switch	14sus	4quadx14x5bit=~320	
QPD whitening + switch	LPOS, LANG, IPPOS, IPANG, TRX, TRY	4quadx6QPDx5bit=120	
SUS dewhitening switch	32(2DACs)*14	448	
Vacuum switch		100	
PEM		100	

*1gain slider uses 16steps=4bit typically, so a 32bit card can handle 4 gain sliders.

1-4-7. DAQ channel list

a. 16kHz (total 64ch)

Part	**Channel point**	**Channel number**	**Description**
Laser	Output laser power [W]	1	
	IFO Input laser power [W]	1	
MC	REFL	1	
	MC length feedback	1	
	MC frequency feedback	1	
OMC	LSC	2	Error, feedback
LSC	I&Q for DARM, CARM, MICH, PRC, SRC, etc.	15	
	error, feedback for DARM, CARM, MICH, PRC, SRC, etc.	15	
SUS	length * 10 suspensions	10	
Calibration		5	

b. 2kHz (total 128ch)

Part	**Channel point**	**Channel number**	**Description**
ASC	WFS	5x4quad x (RF+DC)~50	
	Oplev	14x3(pit, yaw, sum) x ~60	
OMC	ASC	4x2(error, feedback)=8	

c. 256Hz Long term monitor fast (total 512ch)

Part	**Channel point**	**Channel number**	**Description**
Laser	Master laser power [W]	2	
	Output laser power [W]	2	
	IFO Input laser power [W]	2	
Seismic	Room, outside, 3-axis	30	
Tilt meter	Vertex, Main 4 suspensions	5x2~10	Vertex, IX, IY, EX, EY
SUS	Accelerometer	32x14~400	

Sound	Microphone in Room, outside, table	13	3+1(laser room) +5(each PD table), IX, IY, EX, EY, mine

d. 16Hz Long-term monitor slow and Epics channel data (total ~10000ch)

Part	**Channel point**	**Channel number**	**Description**
Temperature [deg.]	Laser crystal temperature [degree] and etc.	10	
	room	10	Vertex, laser, IX, IY, EX, EY, MX, MY
	table	8	Laser, MC, REFL, AS, pickoff x 2, end x 2
	Cryostat	96*4=384	Low temperature
Humidity [%]	rooms	10	Vertex, laser, IX, IY, EX, EY
Dust	rooms	8	Vertex, laser, IX, IY, EX, EY, MX, MY, mine
Air pressure	rooms	8	Vertex, laser, IX, IY, EX, EY, MX, MY, mine
Magnetic field	rooms	8	Vertex, laser, IX, IY, EX, EY, MX, MY, mine
Other EPICS channels	All data recorded by EPICS	10000	center, end, arm

1-4-8. Data transfer rate

	Number of stored channels	Data acquisition, Data analysis, IFO control	16kHz:64ch, 2kHz:512ch, 64Hz:1024ch 16Hz:16384 epics channels (see channel list)	not yet
	Data transfer rate	Data acquisition	4MB/sec for 16kHz, 4MB/sec for 2kHz, 256kB/sec for 64Hz 1MB/sec for 16Hz Total ~10MB/sec ~30GB/hour ~1TB/day ~300TB/year	not yet

1-5. Schedule

Rough schedule is shown in Table 2.

The standalone digital system for subsystems is a part of prototype test and it is based on a lot of experiences at CLIO prototype test, so development of the standalone systems won't be a problem. LCGT will have huge numbers of circuits even for only digital related circuits. We can test how to manage/produce some large numbers of circuits at this stage.

We also do a small network connection test at the same time using 2 or 3 RT control computers, but a whole network connection using many PCs, routers and hubs through metal/fiber cables won't be tested enough until this stage. The first article test would be a very important test as a full network test operation system (TOS) to check enough network speed and stability. This TOS will be moved into mine and be an actual whole network system and a part of RT system.

FY		2010				2011				2012				2013				2014				2015				2016			
Quarter		1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
Main Phase		Design				Tunnel								Vacuum				FPMI		RSE						Cryo			
Prototype test	CLIO operation	■	■	■	■																								
	Data analysys test							■	■	■	■																		
Standalone system for subsystems	Hard/software setup					■																							
	Circuit					■	■	■																					
	Delivery								■																				
Article test	Small network test							■	■																				
	Large network test									■	■	■	■																
Full system installarion	TOS->full system													■	■														
	Software setup														■	■													
	Cuircuits															■	■												
	Newtork																■	■											
Upgrage	RSE																			■	■								
	Cryo																									■	■		

Table 2. Schedule of digital subsystem.

1-6. Prototype Test Plan

Initial basic prototype test for digital system has been performed in Japan using CLIO 100m prototype interferometer in 2009-2010. We succeeded in locking the mass lock loop of CLIO and showed the performance that the noise of ADC and DAC was at least 10times bellower than best sensitivity of CLIO for low temperature operation (shown Fig. 4). We also performed some application technics using the digital system like producing normalized error signals, auto alignment procedures, auto lock procedures and so on. During these experiences, we learned how to obtain required equipment to construct a digital system in Japan with a reasonable price and reasonable term. We are thinking that there is no problem to essentially use aLIGO type digital system in Japan.

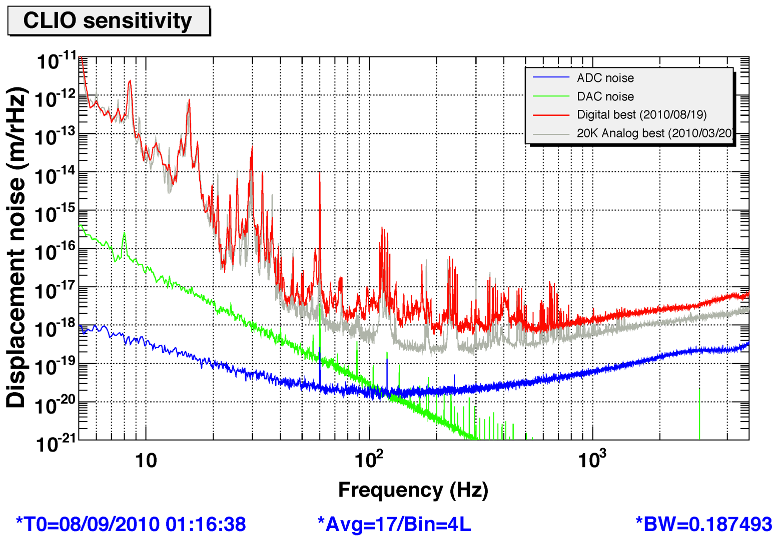

Figure 4. Calibrated CLIO displacement noise using digital system

The main prototype test will be performed in FY 2011 by delivering standalone digital systems to other subgroup. Total 5sets of standalone digital system will be provided from DGS subgroup to other subgroups who need a digital system for development of their subsystems. Following items will be offered to subgroups;

1) Real time control computer as front-end
2) Client workstation PC with software setup
3) PCIe I/O chassis for ADC/DAC/BO modules
4) Timing slave board
5) ADC, DAC, Binary Output
6) Anti Alias/Anti imaging filters

This prototype test can provide a good chance for subgroups to be accustomed to with a digital system before the commissioning of LCGT. It is very important to use and to be familiar with the digital system to extract the performance, so that we hope that new application technics will be invented from other subgroups in not so far future. At the beginning we will offer a typical RT model file for each subsystem and we will have some lectures or instructions in order to explain how to build a RT model and how to use diagnosis/control software.

1-7. First Article Test Plan

We plan to have a test operation system (TOS) with some RT computers and networks as a whole LCGT network. This will be placed in the new Kamioka building in FY2012. This system is independent from actual signal input/output, which means that the TOS has no analog signals and analog circuits like AA/AI filters or interface board. This system consists of following equipment;

1) ~5 RT control computers with I/O chassis
2) ~2 client workstations
3) GPS antenna
4) Timing network with Master /slave timing board
5) DAQ network
6) RFM network
7) PCIe network
8) Fiber connected network routers
9) Several network PCs (1 file server, 1 NTP server, 2 NDS servers, 2-3 DAQ servers)
10) ~3 security and authentication PCs.

Note that multiple computers for NDS and DAQs will be prepared for their redundancy.

1-8. Installation/Adjustment Procedure

Whole test operation system (TOS) will be moved into mine when the installation for digital system starts. Network racks and some of RST racks will be placed into the front room, and most of RTS racks will be moved to the place where each subsystem will be located. Tested network equipment will be located in the corner area and the end rooms, and they will be connected through fibers for 3km arms.

Additionally tested standalone systems that have been used as prototype development for each subsystem will be merged into the whole network. One of the advantages of this installation is what the same model as the standalone system can be used. The number of standalone system may be limited, so additional RT control computers will be installed into the whole system to supplement the required numbers. Needles to say, duplication of the control model from standalone system to new additional RT control computers is quite easy. It may extremely reduce the installation/adjustment time for the installation of all subsystems.
Actual installation will starts with some limited channel numbers for iLCGT and the number of channel will grow for bLCGT, but essentially there is no difference on whole digital system between iLCGT and bLCGT.

1-9. Risk Management

Here is a list of risks of this subsystem.

- Cyber security
  - Probably we need a professional level network security system
- Implementation of timing signal into each RT control computer
  - We will obtain aLIGO timing system via Columbia University.
- Management of huge number of channels
  - Japanese GW group has no experience to deal with such huge channel numbers for order of 1000. Digital system itself is a solution for it but still the number of channels is not small.
- Management of mass production of circuits
  - This is also related to the number of channels. For many channels, selection of cables, connectors and matching the interface to all subsystem are very important.
- Finding problems from too many channels when a trouble happened
  - Sometimes for large computer system, all of the system can be down by only one small trouble. It is very important to have an enough redundancy and to develop a self-diagnostic system.

Since LCGT decided to use aLIGO type digital system, we were relieved a lot of work, for example, selection of ADC/DAC modules, development of real time code, a loop test for control using combined RT control computers, I/O chassises and circuits. First of all, we have to thank LIGO CDS group for offering us such a useful device.

On the other hands, if we do not understand carefully inside the device everything can easily be a black box and very complicated and difficult system to hunt troubles in the future for LCGT construction. Fortunately we have been developed a prototype digital system for CLIO in these 2-3years with LIOG CDS group's corporations and we have experienced many things by constructing several RT control computers from the scratch. These experiences will be a great help for ourselves during the LCGT commissioning.

However it is the fact that we do not have enough experiences for constructing whole network. Technically we knew that the 3km data transfer for real time control which we were concerned about was fixed in LIGO already and we knew that what kind of network equipment we would need to make whole network work properly with enough data transfer speed.

Essentially we do not think we have serious troubles for development of whole digital system for LCGT. Needless to say, this digital subsystem is related to almost of all subsystems, and once a trouble happens on this system it can be a serious delay for the whole LCGT. We continuously should perform reliable operation tests and preparations for the smooth installation and the commissioning of LCGT.

2. Design for iLCGT

2-1. Definition of Subsystem

See section 1-1 on bLCGT.

2-2. Requirements

See section 1-2 on bLCGT.

2-3. Interface

See section 1-3 on bLCGT.

2-4. Final Design

Essentially there is no difference for design of digital subsystem between iLIGO and bLIGO except for channel numbers. At the beginning of iLCGT, the number of channels is very limited, and it will be increased during the development and commissioning of iLCGT and bLCGT.

2-5. Schedule

The whole schedule including for iLCGT and bLCGT is shown in section 1-5 on bLCGT schedule.

2-6. First Article Test Plan

This is explained in section 1-7 as the same as bLCGT first article test plan.

2-7. Installation/Adjustment Procedure

Essentially all digital subsystem components will be installed when iLCGT starts. Installation procedure is explained in section 1-8 on bLCGT.

2-8. Risk Management

See section 1-9 on bLCGT.

Appendix A. Design Match to Requirements

A-1. bLCGT

We estimate the requirement of dynamic range by a typical lock acquisition case and a typical error signal during observation.

1) During lock acquisition, the arm cavity moves ~1um. Finesse of the arm cavity is designed as ~1500, so the full width half maximum (FWHM) is ~1e-9m. When the cavity is locked the motion of cavity should be ~1/1000 of FWHM, so the motion will be roughly 1e-12m. Dynamic range should be > 1e-6m/1e-12m=120dB.

2) Amplitude of error signal during observation can be estimated by an expected seismic motion and a suppression factor by an expected control gain. Typically maximum seismic motion is expected as ~1e-5m/rHz and this low frequency motion is suppressed by a huge control loop gain. The suppression factor can be estimated by an expected unity gain frequency (UGF) = 200Hz and the gain slope of f^-4 between 1Hz and 100Hz, so the suppression factor can be easily obtained as 1e8. On the other hand, target sensitivity expected displacement noise will be 1e-21m/rHz, so the raw dynamic range will be 1e-5m/1e-21m = 1e16 = 320dB, and required dynamic range with the suppression will be 1e16/1e8 = 1e8 = 160dB. Additionally we can use whitening filters which typically consists of 2nd or 4th order of 15Hz-150Hz zero-pole filter, so effectively the whitening filter reduces the required dynamic range by 80dB with 2^{nd} order filter at least. So the assumption of 120dB dynamic range is enough. Note that the power line at 60Hz practically can be a big peak and may limit this dynamic range.

A-2. iLCGT

The same as bLCGT.