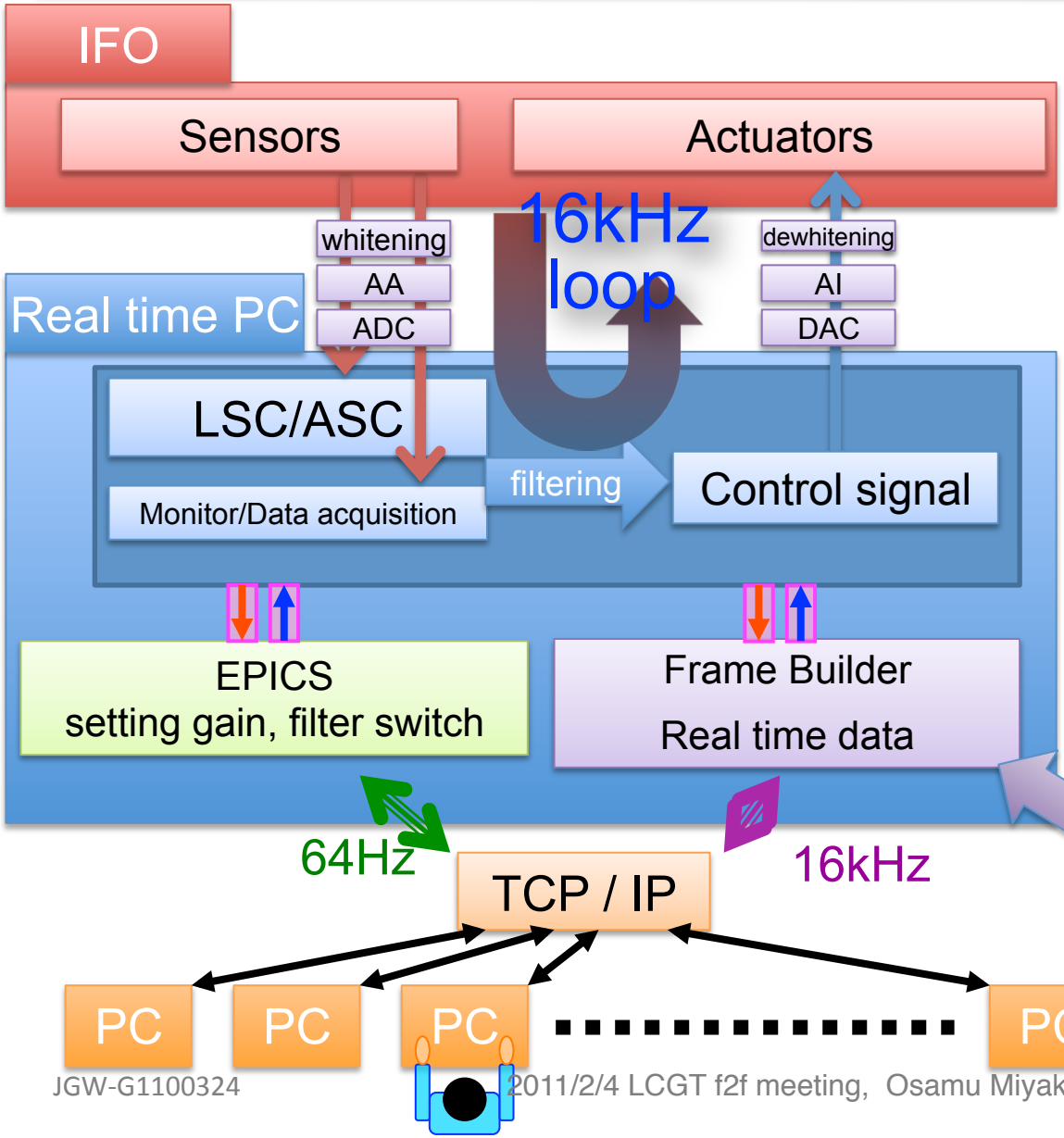
Status report from digital system subgroup

2011/2/4(Fri) LCGT f2f meeting

Osamu Miyakawa, ICRR

Concept of the digital system



- Provides a very flexible human interface to the complex DOFs of the interferometer.
- Functions as sensing, control, monitor, switch
- Good solution to treat huge numbers of signals

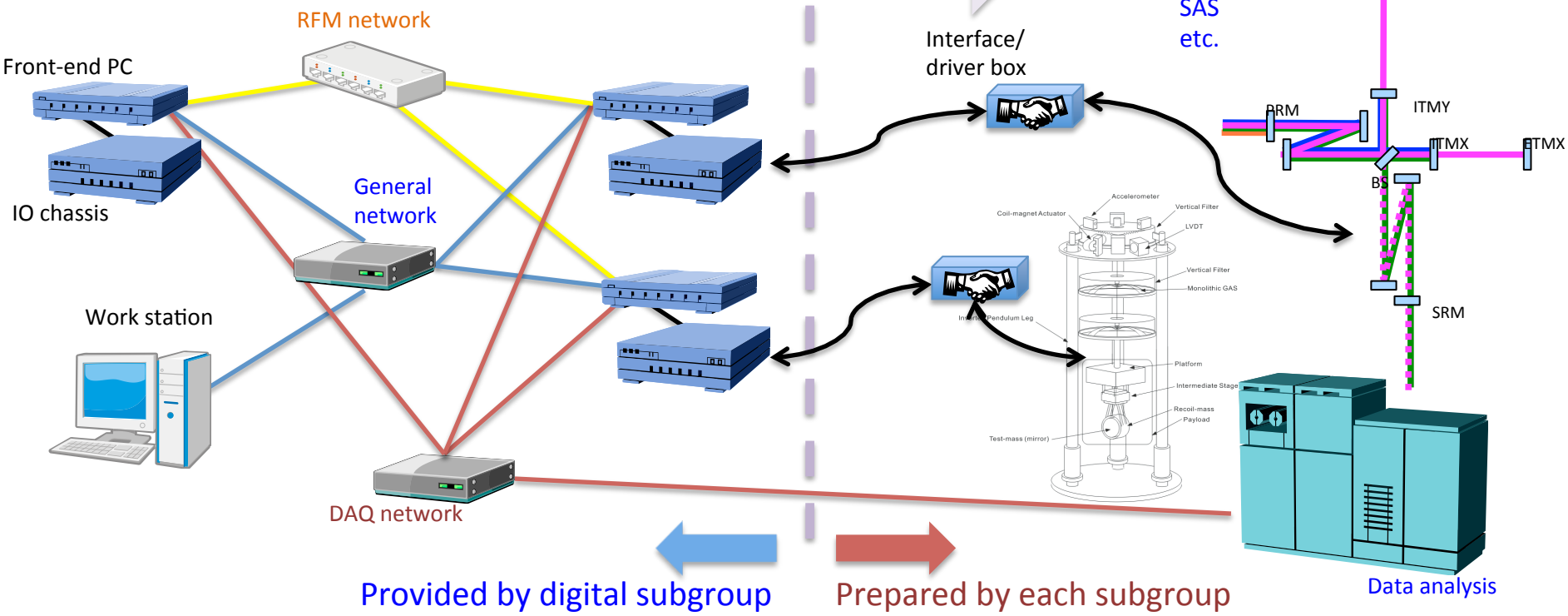
Overview of digital system subgroup

Building digital system with whole network

Providing a platform for signal input/output

Application

Interferometer
SAS
etc.



Provided by digital subgroup

Prepared by each subgroup

- Real time system
- PC, software
- ADC/DAC/BO, AA/AI
- DAQ/RFM/timing network

- Control, monitor, switch
- Auto lock, auto alignment
- Commissioning, noise hunting
- Diagnosis, tuning, calibration
- Operation, observation

Schedule

Before LCGT funded

~FY2010: Development of prototype system at/using CLIO

After LCGT funded

FY2011~: Delivering stand alone system to subgroups

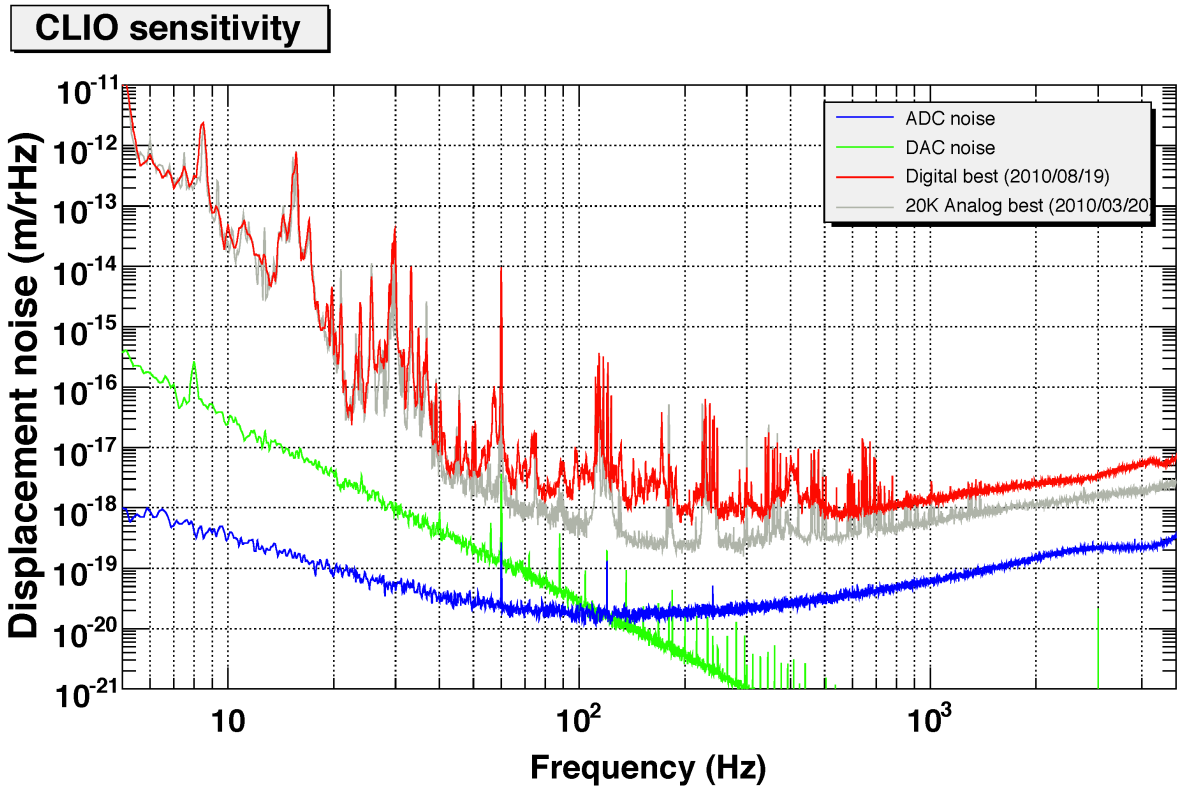
Designing circuits

Small Test bench of network of digital systems

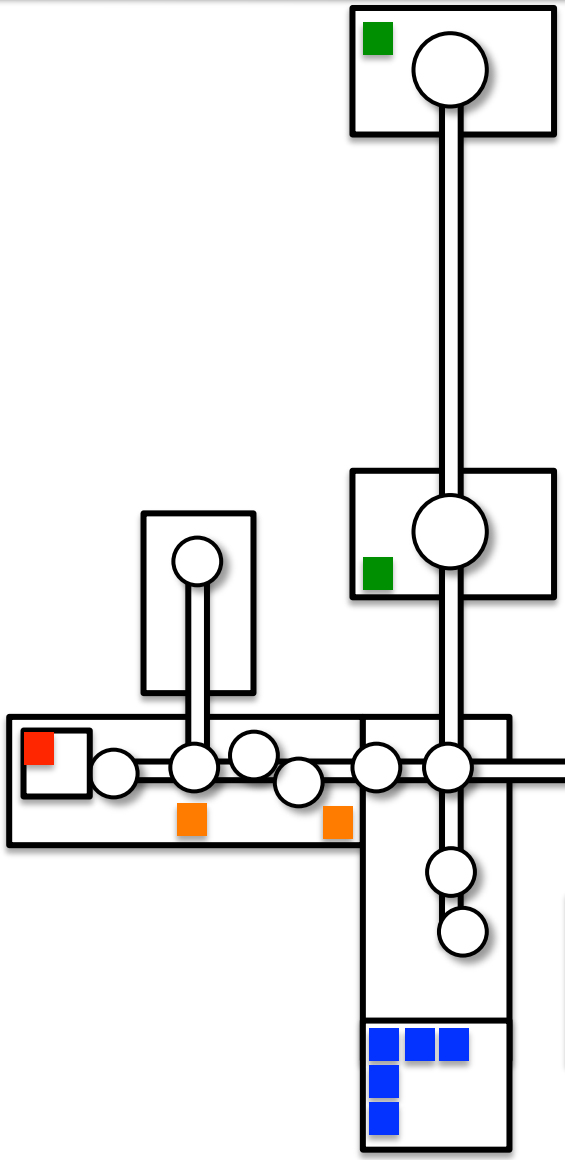
FY2012~: Test operation system as whole network at Kamioka building

FY2013: Installation of full digital system into mine

CLIO sensitivity using Digital control



Hardware



Real time system mounted in 19inch rack: PC, IO chassis (ADC/DAC/BO), timing, AA/AI
- Front room(5): length(1), WFS(2), auxiliary(2)
- Laser room(1): Laser
- Center room(2): Input optics, suspensions
- ITMX(1), ITMY(1)
- ETMX(1), ETMY(1)

Raw data storage at site for 1month long: 100TB

Data storage for iLCGT (analysis, commissioning): 500TB

Data storage for bLCGT: 1PB/year?, not funded

Needs to make a channel list from all subgroups

- Needs whole network design
- Needs network wiring diagram, rack position, rack equipment list

Making channel lists

- Needs channel list for ADC/DAC/BO
  - ADC input ~2048ch
    - will be categorized as class1(IFO main), class2(IFO sub), class3(PEM, physical environment monitor)…
  - DAC output: ~512ch
  - BO: ~2048ch
- DAQ channel: stored signals to data storage as 16kHz, 2kHz, 64Hz…

DAQ Channel list

	Number of stored channels	Data acquisition, Data analysis, IFO control	16kHz:64ch, 2kHz:512ch, 64Hz:1024ch 16Hz:16384 epics channels (see channel list)
*	Data bit resolution at ADC/DAC	Data acquisition	16bit = 65536
*	Data bit resolution in PC	Data acquisition	32bit = 4 Byte integer
	Data transfer rate	Data acquisition	4MB/sec for 16kHz, 4MB/sec for 2kHz, 128kB/sec for 64Hz, 1MB/sec for 16Hz, Total ~10MB/sec ~30GB/hour ~1TB/day ~300TB/year

6. Channel list

a. 16kHz (total 64ch)

Part	Channel point	Channel number	Description
Laser	Output laser power[W]	1	
	IFO Input laser power[W]	1	
MC	REFL	1	
	MC length feedback	1	
	MC frequency feedback	1	
LSC	I&Q dor DARM, CARM, MICH, PRC, SRC, etc.	10	
	error, feedback	10	
SUS	length * 10 suspensions	10	

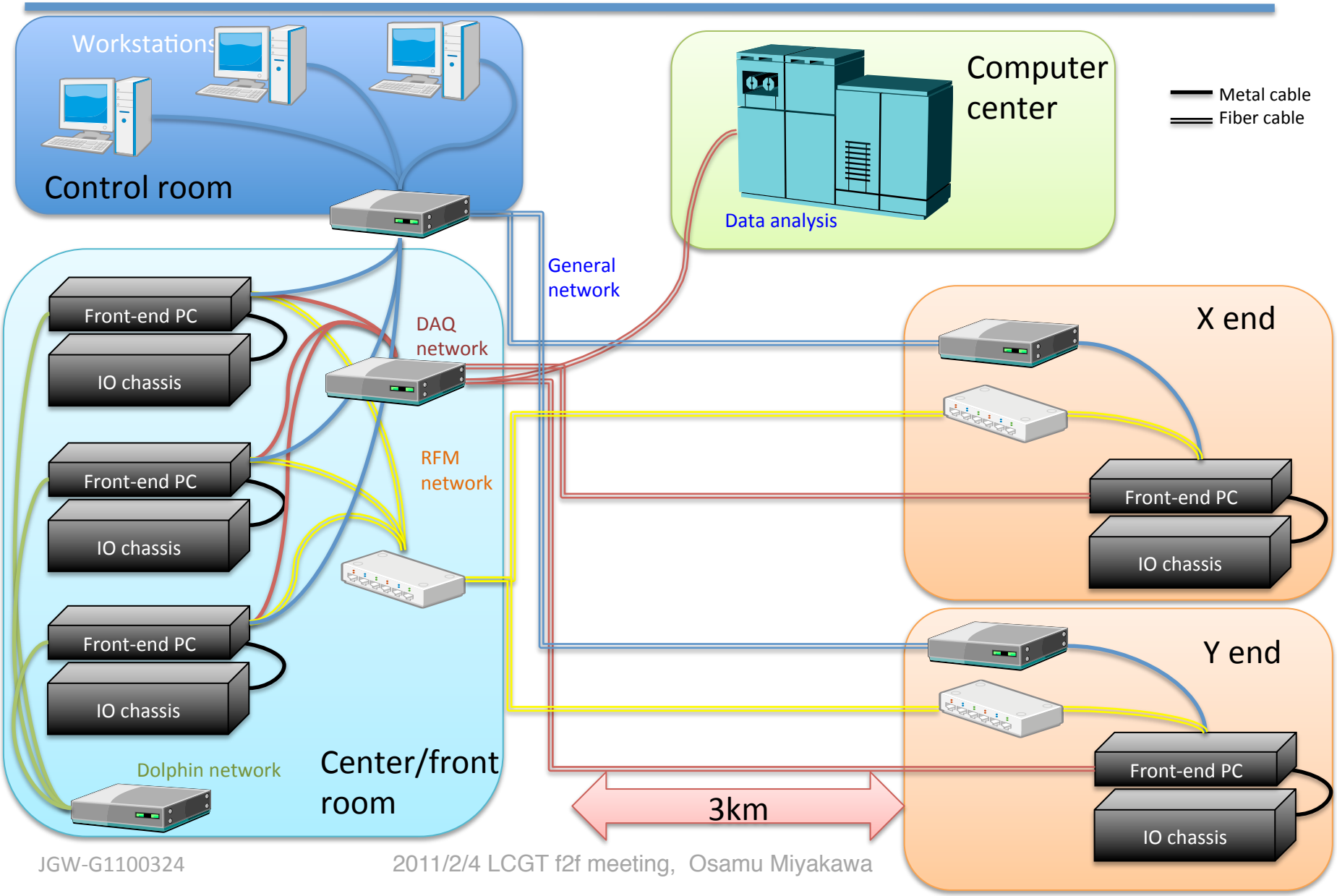
b. 2kHz (total 256ch)

Part	Channel point	Channel number	Description
ASC	WFS	5xpitch, yaw=50	
	Oplev	10xpitch,yaw=100	

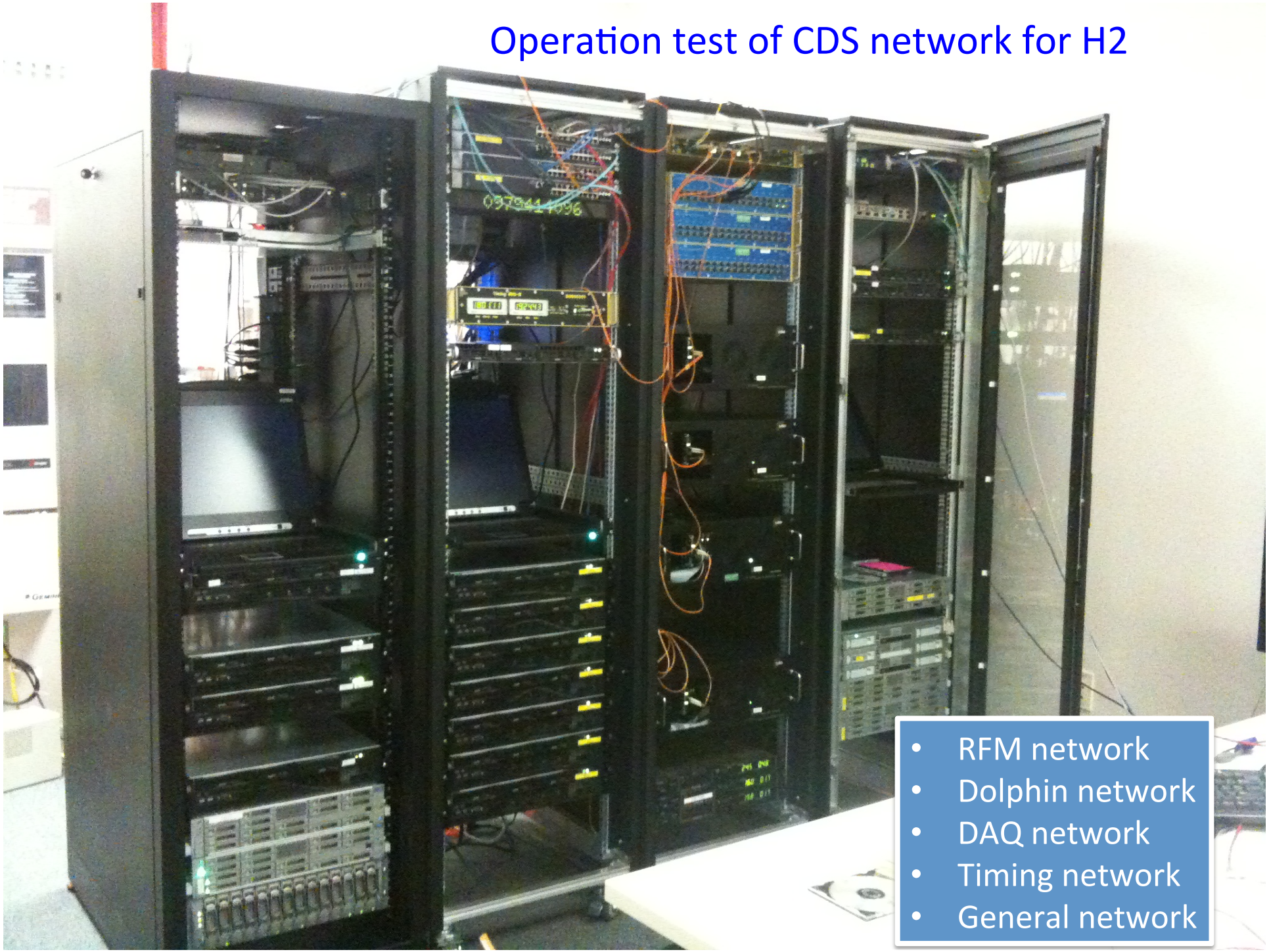
c. 64Hz Long term monitor (total 512ch)

Part	Channel point	Channel number	Description
Temperature[deg]	room	10	center, end, arm
	table	10	laser, REFL, AS, pickoff, end
	suspensions	50	Low temperature
	mirrors	50	Low temperature
Humidity[%]	rooms	10	center, end, arm
Dust	rooms	10	center, end, arm
Laser	crystal temperature[degree] and etc.	10	
	Master laser power[W]	2	

Network design



Operation test of CDS network for H2



- RFM network
- Dolphin network
- DAQ network
- Timing network
- General network

Connecting subsystems into digital system

Front-end PC
- Real time core

Network router

Workstation
- Dataviewer(oscilloscope)
- DTT(FFT)
- Foton(digital filter setting)

IO chassis

ADC DAC BO

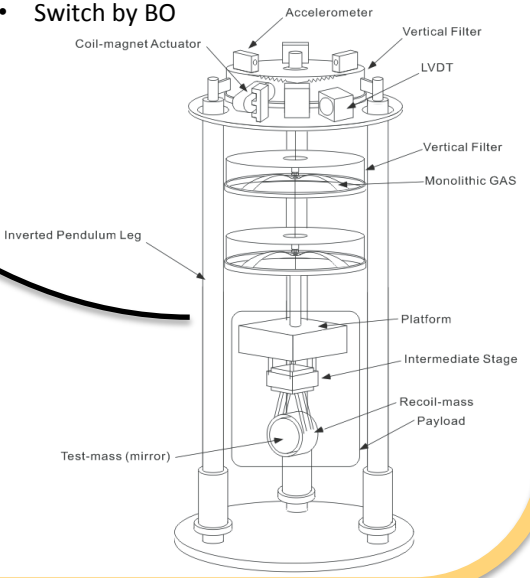
Prepared by each subgroup

Interface/driver box
- Variable gain stage
- Whitening
- dewhitening filter
- Switch by BO

Anti Alias filter box

Anti Imaging filter box

Binary Output interface box



:D-sub connector

Stand alone system for subsystems

- 5sets of stand alone digital system will be delivered to subgroups in FY2011
  - Front-end real time PC
  - Workstation/desktop PC with software setup
  - Expansion chassis
  - Timing slave board
  - ADC, DAC, Binary Output
  - Interface board to ADC/DAC/BO
  - Anti Alias/Anti imaging

- Seismic attenuation, IOO group, cryostat…
- Budget:
  - 21M yen in FY2010 for PC, IO chassis, ADC/DAC and other hardware(almost done)
  - 15M yen in GY2011 for circuits

Interface

- ADC 32ch/card
  - 16kHz sampling
  - With Anti Alias filters
  - 2uV/rHz
  - D-sub 9pin(for 4ch, differential), +/-20V input
- DAC 16ch/card
  - With Anti Imaging filers
  - 1.5uV/rHz
  - D-sub 9pin(for 4ch, differential), +/-10V output
- BO 32ch/card
  - D-sub 9pin(for 4ch, differential), 0 or +5V output
    - Ex. Variable gain amp for 16 steps/1 D-sub connector

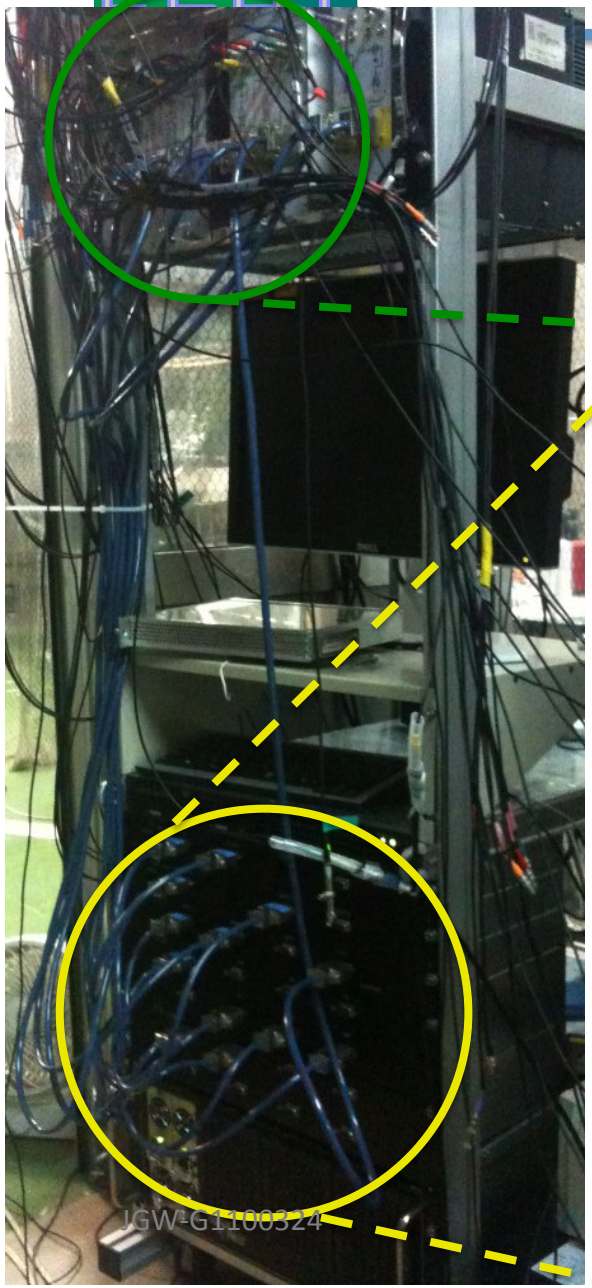
Designing subsystems with digital system

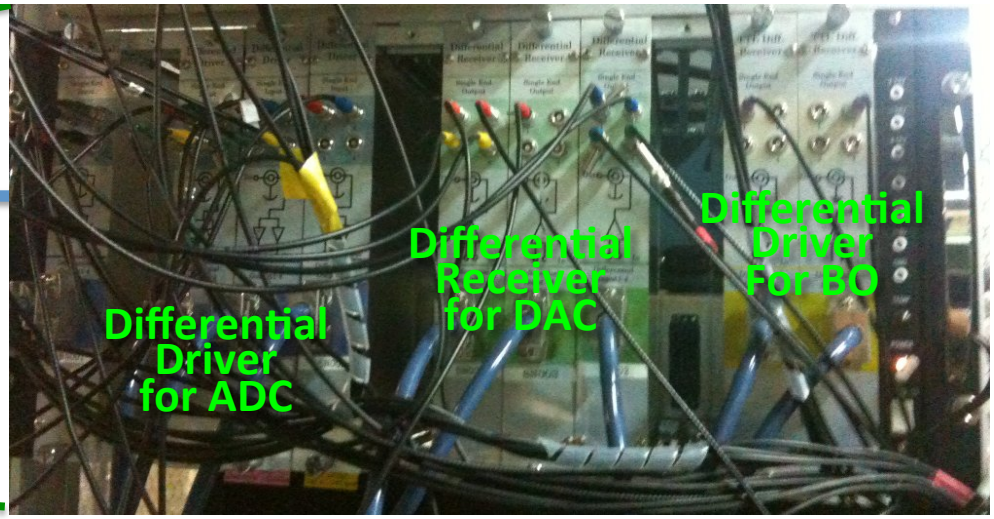
- Include following items on your subsystem's design;
  - Analog variable gain stage
  - Analog Whitening/dewhitening filters
  - BO switch for stepping gain stage and switching w/dw filters on/off
  - Do NOT contain slow analog servo, make it digital! We will offer enough number of channels

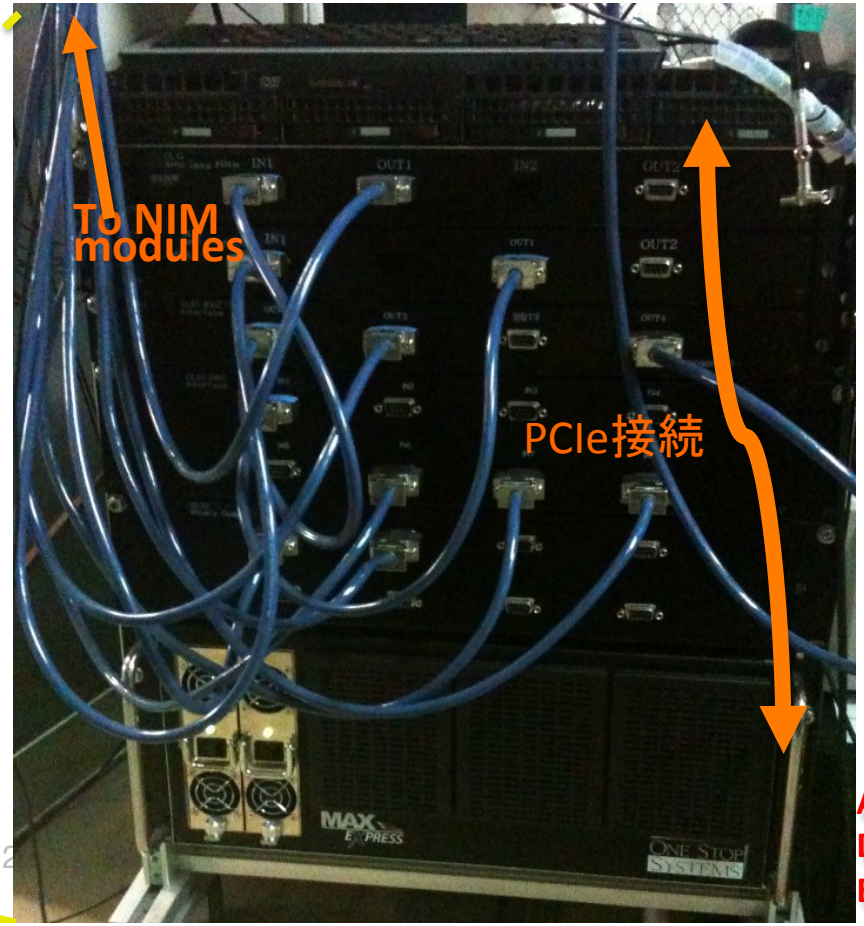
- Make a Driver/interface box between your subsystem and digital system to realize above functions

- Propose 100V/rHz rule:
  - Do NOT transfer under 100nV/rHz signal, too fragile
  - Amplifier signals until over 100nV/rHz before transfer
  - Use analog variable gain stage and whitening filters in your box which is controlled by digital BO

Pictures







Real time PC
CentOS 5.2+real time kernel
4core x 2 Xeon

Anti Imaging filters
Anti Alias filters

DAC adapter

ADC adapter

Binary output adapter

ADC/DAC
In Expansion Chassis

ADC:32ch/$4K
DAC:16ch/$3.5K
Binary Output:32ch/$250

Client system